

PCN Number: RC140702

Notification Date*: April 3, 2014

Title: Migration to Marketing Revision Level B of the AT91SAM7SE512 and AT91SAM7SE256

Product Identification:

Current Part Number	New Part Number
AT91SAM7SE256-AU	AT91SAM7SE256B-AU
AT91SAM7SE256-AU-999	AT91SAM7SE256B-AUR
AT91SAM7SE256-CU	AT91SAM7SE256B-CU
AT91SAM7SE256-CU-999	AT91SAM7SE256B-CUR
AT91SAM7SE512-AU	AT91SAM7SE512B-AU
AT91SAM7SE512-AU-999	AT91SAM7SE512B-AUR
AT91SAM7SE512-CU	AT91SAM7SE512B-CU
AT91SAM7SE512-CU-999	AT91SAM7SE512B-CUR

Reason for Change:

- | | |
|--|--|
| <input type="checkbox"/> Material / Composition | <input checked="" type="checkbox"/> Manufacturing Location |
| <input checked="" type="checkbox"/> Processing / Manufacturing | <input type="checkbox"/> Quality / Reliability |
| <input checked="" type="checkbox"/> Design / Firmware | <input checked="" type="checkbox"/> Logistics |
| <input checked="" type="checkbox"/> Datasheet | <input type="checkbox"/> Other: |

Change Description:

A complete list of differences between the marketing revision level (MRL) A and B can be found in chapter 43 of the AT91SAM7SE series datasheet with Atmel document reference 6222H.

Multiple errata have been corrected on the ADC, PWM, RTT, SPI, SSC, TWI and USART.

The rev B is manufactured in 0.15micron embedded Flash technology at UMC.

The ChipID has been incremented to:

AT91SAM7SE512 Revision B chip ID is 0x272A 0A41

AT91SAM7SE256 Revision B chip ID is 0x272A 0941

The number of Flash Wait States (FWS) according to the frequency requirements has changed. Please refer to the section 43.3.2.1 EFC : Embedded Flash Access Time of the datasheet (6222H).

Embedded Flash Wait State VDDCORE set at 1.65V

Flash Wait State	Read Operations	Maximum Operating Frequency (MHz)
0	1 cycle	20
1	2 cycles	40
2	3 cycles	48.2
3 ⁽¹⁾	4 cycles	48.2

Notes:

1. It is not necessary to use 3 wait states because the Flash can operate at maximum with only 2 wait states.

Embedded Flash Wait State VDDCORE set at 1.80V

Flash Wait State	Read Operations	Maximum Operating Frequency (MHz)
0	1 cycle	21.5
1	2 cycles	43
2	3 cycles	55
3 ⁽¹⁾	4 cycles	55

Notes:

1. It is not necessary to use 3 wait states because the Flash can operate at maximum with only 2 wait states.

Samples are available in Atmel Sample Center:

<https://samples.atmel.com/scripts/samplecenter.dll?atmel?cmd=menu>

Identification Method to Distinguish Change:

Marketing Revision Level (MRL) has been incremented on the top side marking to B

Qualification Data:	<input checked="" type="checkbox"/> Available	<input type="checkbox"/> Will be available (mm/dd/yr):	<input type="checkbox"/> Not Applicable
Samples:	<input checked="" type="checkbox"/> Available	<input type="checkbox"/> Will be available (mm/dd/yr):	<input type="checkbox"/> Not Applicable

Quantifiable Impact on Quality & Reliability:

None

Forecasted Availability Date: March 31, 2014

Last Time Buy Date: March 31, 2014

Last Ship Date: March 31, 2015

**All orders placed after the notification date are non-cancellable and non-returnable (NCNR).*

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