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4-Bit 100 Mb/s Configurable **Dual-Supply Level Translator**

NLSX5004, NLSXN5004

The NLSX5004 and NLSXN5004 are 4-bit configurable dual-supply autosensing bidirectional level translators that do not require direction control pins. The A- and B-ports are designed to track two different power supply rails, V_{CCA} and V_{CCB} respectively. Both the V_{CCA} and the V_{CCB} supply rails are independentlyconfigurable from 0.9 V to 3.6 V.

The NLSX5004 and NLSXN5004 have high dynamic output current capability, allowing the translators to drive high capacitive loads.

Enable input pins are available to reduce the power consumption. These pins may be used to disable both A- and B-ports by putting them in 3-state significantly reducing the supply current from both V_{CCA} and V_{CCB}. These pins are referenced to the V_{CCA} supply. The NLSX5004 has an active-High enable (EN) while the NLSXN5004 has active-Low enable (\overline{EN}) .

Features

- Wide V_{CCA}, V_{CCB} Operating Range: 0.9 V to 3.6 V
- V_{CCA} and V_{CCB} are independent
 - V_{CCA} may be greater than, equal to, or less than V_{CCB}
- High 100 pF Capacitive Drive Capability
- High-Speed w/ 140 Mbps Guaranteed Date Rate for V_{CCA}, $V_{CCB} > 1.8 \text{ V}$
- Low Bit-to-Bit skew
- Overvoltage Tolerant Enable and I/O Pins
- Non-preferential Power-Up Sequencing
- Partial Power-Off Protection
- Available packaging:
 - UQFN-12, SOIC14, TSSOP14, QFN-14, Other packages
- NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable
- These Devices are Pb-Free, Halogen Free/BFR Free and RoHS Compliant

Typical Applications

• Mobile Phones, Infotainment Systems, Other Devices

Important Information

• ESD Protection for All Pins: HBM (Human Body Model) - 2000 V



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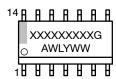
www.onsemi.com



UQFN12 **MU SUFFIX** CASE 523AE



D SUFFIX CASE 751A



14 888888

XXXX

XXXX ALYW.

MARKING DIAGRAMS

A2M



TSSOP14 **DT SUFFIX CASE 948G**





QFN14 **MN SUFFIX** CASE 485AL



XXXX

AYW

XXXXX = Specific Device Code

= Date Code = Assembly Location

L or WL = Wafer Lot = Year

W or WW = Work Week G or ■ = Pb-Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering and shipping information on page 11 of this data sheet.

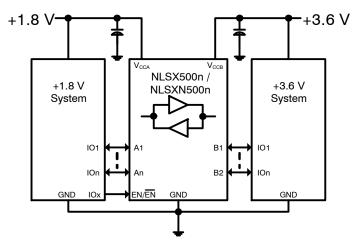


Figure 1. Typical Application Circuit

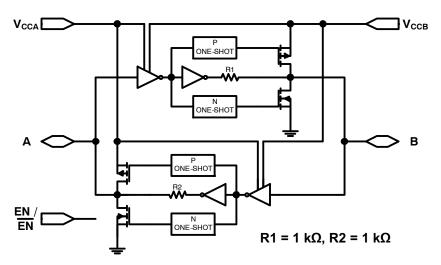


Figure 2. Functional Diagram (1 I/O Line)

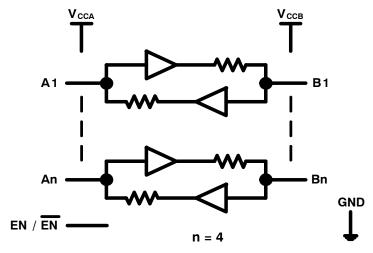


Figure 3. Logic Diagram

PIN ASSIGNMENTS

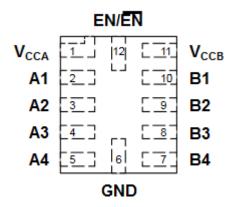


Figure 4. UQFN12

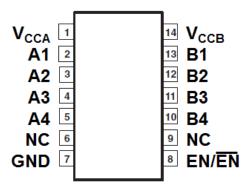


Figure 6. TSSOP / SOIC

PIN DESCRIPTIONS

Pins	Description
V _{CCA}	A-Port Supply Voltage
V _{CCB}	B-Port Supply Voltage
GND	Ground
EN	Active-High Enable (NLSX500n), Referenced to V _{CCA}
ĒN	Active-Low Enable (NLSXN500n), Referenced to V _{CCA}
An	A-Port, Referenced to V _{CCA}
Bn	B-Port, Referenced to V _{CCB}

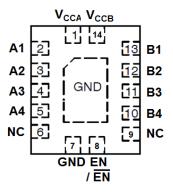


Figure 5. QFN14 (2.5 x 3.0)

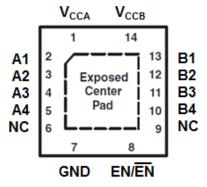


Figure 7. QFN14 (3.5 x 3.5)

FUNCTION TABLE

NLSX500n	NLSXN500n	Operating			
EN	EN	Mode			
L	Н	An and Bn at Hi–Z			
Н	L	An and Bn Connected			

Table 1. MAXIMUM RATINGS

Symbol	Parameter		Value	Condition	Unit
V _{CCA}	A-side DC Supply Voltage	/ Voltage			V
V _{CCB}	B-side DC Supply Voltage		-0.5 to +4.6		V
V _{IN}	Input/Output Voltage	EN/EN	-0.5 to +4.6		V
	Power Down Mode (V _{CCA} and/or	Power Down Mode (V _{CCA} and/or V _{CCB} = 0 V)			
	Tri-State Mode (EN = I	or EN = H)	-0.5 to +4.6		
	Active Mode	A-Port	-0.5 to V _{CCA} +0.5		
		B-Port	-0.5 to V _{CCB} +0.5		
I _{IK}	DC Input Diode Current		-50	V _{IN} < GND	mA
I _{OK}	DC Output Diode Current		-50	V _O < GND	mA
I _{CCA}	DC Supply Current Through V _{CCA}		±100		mA
I _{CCB}	DC Supply Current Through V _{CCB}	nrough V _{CCB}			mA
I _{GND}	DC Ground Current Through Ground Pin	nrough Ground Pin			mA
T _{STG}	Storage Temperature		-65 to +150		°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

Table 2. RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
V _{CCA}	A-Port Supply Voltage		0.9	3.6	V
V _{CCB}	B-Port Supply Voltage		0.9	3.6	V
VI	Input/Output Voltage	EN/EN	GND	3.6	V
	Power Down Mode (V _{CCA} and/or \	/ _{CCB} = 0 V)	GND	3.6	
	Tri-State Mode (EN = L	or EN = H)	GND	3.6	
	Active Mode	A-Port	GND	V _{CCA}	
		B-Port	GND	V _{CCB}	
T _A	Operating Temperature Range		-40	+125	°C
Δt/ΔV	Input Transition Rise or Fall Rate V _I from 30% to 70% of V _{CCA} /V _{CCB}		0	10	nS

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

Table 3. DC ELECTRICAL CHARACTERISTICS

						-40	0°C to +85	5°C	-40°C to	+125°C	
Symbol	Parameter	Test Conditions (Note 1)	Pin/Port	V _{CCA} (V)	V _{CCB} (V)	Min	Typ (Note 2)	Max	Min	Max	Unit
V _{IH}	Input HIGH Voltage		A, EN/EN	0.9–3.6	0.9–3.6	0.65 * V _{CCA}	-	-	0.65 * V _{CCA}	-	V
			В	0.9–3.6	0.9-3.6	0.65 * V _{CCB}	-	-	0.65 * V _{CCB}	-	V
V _{IL}	Input LOW Voltage		A, EN/EN	0.9–3.6	0.9-3.6	-	-	0.35 * V _{CCA}	-	0.35 * V _{CCA}	V
			В	0.9–3.6	0.9-3.6	_	-	0.35 * V _{CCB}	-	0.35 * V _{CCB}	V
V _{OH}	Output HIGH Voltage	I _{OH} = -20 μA	А	0.9–3.6	0.9-3.6	0.9 * V _{CCA}	-	-	0.9 * V _{CCA}	-	V
			В	0.9–3.6	0.9–3.6	0.9 * V _{CCB}	-	-	0.9 * V _{CCB}	-	V
V _{OL}	Output LOW	I _{OL} = 20 μA	Α	0.9–3.6	0.9–3.6	-	-	0.2	-	0.2	V
	Voltage		В	0.9–3.6	0.9–3.6	_	-	0.2	-	0.2	V
l _{OZ}	Tristate Output	(EN = 0V or $\overline{\text{EN}} = V_{\text{CCA}}$);									μА
	Leakage	(A = 0 V or V _{CCA})	Α	0.9–3.6	0.9–3.6	-	0.01	±1.5	-	±4.5	
		(B = 0 V or V _{CCB})	В	0.9–3.6	0.9–3.6	_	0.01	±1	-	±3.5	
I _I	Input Pin Leakage	V _{IN} = 0 V to V _{CCA}	EN/EN	0.9–3.6	0.9–3.6	-	0.01	±1	-	±3	μΑ
I _{CC}	Supply Current	$(EN = V_{CCA} \text{ or } \overline{EN} = 0 \text{ V});$	V _{CCA}	0.9–3.6	0.9–3.6	-	0.4	2.0	-	6.0	μΑ
		$I_O = 0 \text{ A}, (A = 0 \text{ V}, B = 0 \text{ V})$ or $(A = V_{CCA}, B = V_{CCB})$	V _{CCB}	0.9–3.6	0.9–3.6	_	0.3	1.5	-	6.0	
I _{CCZ}	Tristate Output	(EN = 0V or $\overline{\text{EN}}$ = V _{CCA}),	V _{CCA}	0.9–3.6	0.9–3.6	-	0.2	1.5	-	7.0	μА
	Mode Supply Current	(A = 0 V, B = 0 V) or $(A = V_{CCA}, B = V_{CCB})$	V _{CCB}	0.9-3.6	0.9-3.6	_	0.2	1.5	_	6.0	
l _{OFF}	Power Off	A = 0 to 3.6 V,	A, B	0	0	-	0.02	1.5	-	5.0	μΑ
	Leakage	B = 0 to 3.6 V		0.9–3.6	0	-	0.01	1.5	-	5.0	
				0	0.9–3.6	-	0.01	1.5	-	5.0	

 Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.
 Normal test conditions are V_I = 0 V, C_{LA} ≤ 15 pF and C_{LB} ≤ 15 pF, unless otherwise specified.
 Typical values are for T_A = +25°C. All units are production tested at T_A = +25°C. Limits over the operating temperature range are guaranteed by design. Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product

Table 4. TIMING CHARACTERISTICS

Symbol Parameter Test Conditions (Note 3)							-4	0°C to +85	5°C	-40°C to	+125°C	
Propagation Delay For Degration Delay CL = 50 pF Rep Propagation Delay Rep Propagation Delay CL = 50 pF Rep Propa	Symbol	Darameter	Test Conditions (N	ote 3)	V (/)	V (/)	Min		Max	Min	Max	Unit
$t_{PD} = \text{Propagation Delay} \\ c_{L} = 50 \text{pF} \\ \hline \\ c_{L} = 50 $	Cymbol	1 didilicter	rest conditions (iv	T								Oiiit
A to B												
From pagation Delay Propagation Delay CL = 30 pF CL = 50 pF A to B 18												
Republic Propagation Delay Fig. 1 = 50 pF A to B 2.8												
C _L = 15 pF C				A to B								
C _L = 15 pF										-		
Region Delay C _L = 15 pF Region Delay C _L = 50 pF Region Delay Reg							_			_		
tpD Propagation Delay CL = 30 pF CL = 50							_			_		
Propagation Delay Propagation Delay Propagation Delay CL = 30 pF Propagation Delay CL = 50 pF C			$C_L = 15 pF$				_			-		
## B to A 1.8							_	9.9	12	_		
B to A 1.8							_	7.3		_		
Record R					1.8		-	5.8	7.5	-	7.5	
## The composition of the compos				B to A	2.8	1.8	_	4.9	7	-	7	
tpD Propagation Delay CL = 30 pF Eq. (a) Fig. 1.8					1.8	3.3	-	5.7	7	-	7	
Propagation Delay CL = 30 pF CL = 50 pF R to B A to B O.9-3.6					3.3	1.8	_	4.6	6	-	6	
The propagation Delay $C_L = 30 \mathrm{pF}$ and $C_L = 30 \mathrm{pF}$ $C_L =$					1.8–3.6	1.8-3.6	_	4.3	9.5	-	10	
$t_{PD} \ \ \text{Propagation Delay} \ \ C_L = 30 \text{pF} \ \ \begin{array}{c ccccccccccccccccccccccccccccccccccc$					0.9–3.6	0.9–3.6	_	9.1	32	-	35	
$t_{PD} = t_{PD} = t$					1.2	1.8	_	7.8	9.3	-	9.3	
Propagation Delay CL = 30 pF CL = 30 pF CL = 30 pF CL = 30 pF A to B 2.8				A to B	1.8	1.2	-	10.8	12.6	-	12.6	
Propagation Delay CL = 30 pF CL = 30 pF CL = 30 pF CL = 30 pF Respond to the propagation Delay CL = 30 pF CL = 30 pF CL = 30 pF Respond to the propagation Delay CL = 30 pF Respond to the propagation Delay CL = 30 pF Respond to the propagation Delay CL = 30 pF Respond to the propagation Delay CL = 30 pF Respond to the propagation Delay CL = 30 pF Respond to the propagation Delay CL = 30 pF Respond to the propagation Delay CL = 30 pF Respond to the propagation Delay CL = 30 pF Respond to the propagation Delay CL = 30 pF Respond to the propagation Delay					1.8	2.8	_	6.2	7.4	-	7.4	
Propagation Delay CL = 30 pF CL = 30 pF Residue Section Sec					2.8	1.8	_	6.0	7.9	-	7.9	- - -
Propagation Delay CL = 30 pF Representation Delay CL = 30 pF Representation Delay CL = 30 pF Representation Delay Representat					1.8	3.3	_	6.1	7.4	-		
Propagation Delay CL = 30 pF B to A B to A B to A CL = 50 pF CL = 50 pF CL = 50 pF CL = 50 pF R to A B to A						1.8	_	4.2	6.5	-	6.5	
B to A B to A B to A CL = 50 pF 1.9	too	Propagation Delay	C ₁ = 30 pF				_			-		ne
CL = 50pF	4PD	1 Topagation Belay	OL = 30 PF				-			-		-
A T B T A A B T A A A A A A A A							-			-		
$ C_{L} = 50pF $							_			-		
$C_{L} = 50 \text{pF}$				B to A			_			-		
$CL = 50pF$ $\begin{array}{ c c c c c c c c c c c c c c c c c c c$				2 10 71			_			-		
$C_{L} = 50 \text{pF}$												
$C_{L} = 50pF$ F $AtoB$ $BtoA$ AB $BtoA$ AB AIB AIB AIB AIB AIB AIB AB $ABBBA$ $ABBBA$ $ABBBA$ $ABBBBA$ $ABBBBA$ $ABBBBA$ $ABBBBA$ $ABBBBB$ $ABBBBBBBB$												
$C_{L} = 50 \text{pF}$ $\begin{array}{c ccccccccccccccccccccccccccccccccccc$												
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$C_{L} = 50 \text{pF}$ $\begin{array}{c ccccccccccccccccccccccccccccccccccc$				A to B								
$C_{L} = 50 \text{pF}$												
$C_{L} = 50 \text{ pF} \\ \hline \\ B \text{ to A} \\ B \text{ to A} \\ \hline \\ B \text{ to A} \\ \hline \\ \hline \\ B \text{ to A} \\ \hline \\ \hline \\ \hline \\ B \text{ to A} \\ \hline \\ \hline \\ \hline \\ \hline \\ B \text{ to A} \\ \hline \\ $												
C _L = 50 pF 0.9-3.6												
B to A 1.2 1.8 - 11.1 13.6 - 13.6 1.8 1.2 - 8.1 9.5 - 9.5 1.8 2.8 - 2.8 1.8 - 1.8			C _L = 50 pF									
B to A 1.8												
B to A												
B to A 2.8 1.8 - 6.5 7.6 - 7.6 1.8 3.3 - 4.3 6.6 - 6.6 3.3 1.8 - 6.3 7.6 - 7.6												
1.8 3.3 - 4.3 6.6 - 6.6 3.3 1.8 - 6.3 7.6 - 7.6				B to A								
3.3 1.8 - 6.3 7.6 - 7.6												
					1.8–3.6	1.8–3.6	_	4.7	10.3	_	10.8	

^{3.} Typical values are for $T_A = +25^{\circ}C$. Limits over the operating temperature range are guaranteed by design. 4. Guaranteed by design.

Table 4. TIMING CHARACTERISTICS (continued)

	TIMING OFFICE					-4	0°C to +8	5°C	-40°C to	+125°C						
Symbol	Parameter	Test Conditions (No	ote 3)	V _{CCA} (V)	V _{CCB} (V)	Min	Typ (Note 4)	Max	Min	Max	Unit					
				0.9–3.6	0.9–3.6	-	9.9	-	-	-						
				1.2	1.8	_	8.4	10	_	10						
				1.8	1.2	_	11.5	14	_	14						
			A 1 - D	1.8	2.8	-	5.5	8.3	-	8.3						
			A to B	2.8	1.8	-	6.9	8.9	-	9.0						
				1.8	3.3	-	5.1	6.7	-	6.8						
				3.3	1.8	-	6.8	8.2	-	8.2						
1	Dunnanting Dalace	0 400 - 5		1.8–3.6	1.8–3.6	_	5.0	11	_	11.5						
t _{PD}	Propagation Delay	C _L = 100 pF		0.9-3.6	0.9-3.6	_	9.9	-	_	_	ns					
				1.2	1.8	-	11.5	14	-	14						
				1.8	1.2	-	8.4	10	-	10						
			D	1.8	2.8	-	6.9	8.9	-	9.0						
			B to A	2.8	1.8	-	5.5	8.3	-	8.3						
				1.8	3.3	-	6.8	8.2	_	8.2						
				3.3	1.8	-	5.1	6.7	-	6.8						
				1.8–3.6	1.8–3.6	-	5.0	11	_	11.5						
				0.9–1.2		_	2.5	4.5	_	4.5						
				1.2–1.8		_	2.0	3.0	_	3.0						
			Α	1.8–2.8	0.9–3.6	_	0.6	2.0	_	2.0						
	t _R Output Rise Time trial			2.8-3.6		-	0.5	2.5	_	2.5	-					
t _R		C _L = 15 pF			0.9–1.2	_	2.5	4.5	_	4.5	ns					
					1.2–1.8	_	2.0	3.0	_	3.0						
			В	0.9–3.6	1.8–2.8	_	0.6	2.0	_	2.0						
					2.8–3.6	_	0.5	2.5	_	2.5						
				0.9–1.2		-	2.5	6.0	_	6.0						
			1.2–1.8		_	1.8	3.0	_	3.0							
			Α	A 1.8–2.8 2.8–3.6	0.9–3.6	_	0.6	2.0	_	2.0	1					
						_	0.5	2.5	_	2.5						
t _F	Output Fall Time trial	C _L = 15 pF			0.9–1.2	-	2.5	6.0	_	6.0	ns					
										1.2–1.8	_	1.8	3.0	_	3.0	
			В	0.9–3.6	1.8–2.8	_	0.6	2.0	_	2.0						
					2.8–3.6	-	0.5	2.5	_	2.5						
tsĸ	Channel-to-Channel Skew			0.9–3.6	0.9–3.6	-	-	0.15	-	0.15	ns					
			I	0.9–3.6	0.9–3.6	50	_	_	50	_						
		C _L = 15 pF		1.8–3.6	1.8–3.6	140	_	_	140	_						
				0.9–3.6	0.9–3.6	40	_	_	40	_						
		C _L = 30 pF		1.8–3.6	1.8–3.6	120	_	_	120	_						
MDR	Maximum Data Rate			0.9–3.6	0.9-3.6	30	_	_	30	_	Mbps					
		C _L = 50 pF		1.8–3.6	1.8–3.6	100	_	_	100	-	-					
					0.9–3.6	20	_	_	20	_	1					
		C _L = 100 pF		0.9–3.6 1.8–3.6	1.8-3.6	60	_	_	60	-						
		$\frac{EN}{EN} = V_{CCA} \text{ or } $ $EN = 0 \text{ V}$		<u> </u>			1		<u> </u>							
I _{I_PEAK}	Input Driver Peak Current	A = 1 MHz Sq Wave, Amplitude = V _{CCA}	Α	0.9–3.6	0.9–3.6	-	_	5.0	_	5.0	mA					
		B = 1 MHz Sq Wave, Amplitude = V _{CCB}	В	0.9–3.6	0.9–3.6	-	-	5.0	_	5.0	1					

Typical values are for T_A = +25°C. Limits over the operating temperature range are guaranteed by design.
 Guaranteed by design.

Table 4. TIMING CHARACTERISTICS (continued)

						-40	0°C to +8	5°C	-40°C to	+125°C												
Symbol	Parameter	Test Conditions (No	ote 3)	V _{CCA} (V)	V _{CCB} (V)	Min	Typ (Note 4)	Max	Min	Max	Unit											
				0.9		-	37	-	-	-												
			Α	1.8	0.9-3.6	-	20	_	-	-												
Z _O	1-Shot Output			3.6		-	10	-	-	-	Ω											
(Note 4)	Impedance				0.9	ı	37	1	_	i	22											
			В	0.9–3.6	1.8	ı	20	1	-	ı												
					3.6	ı	10	1	-	ı												
				0.9–3.6	0.9–3.6	ı	116.3	200	_	200												
		C _L = 15 pF; B = V _{CCB}		1.2–1.8	1.2–1.8	ı	64.5	180	_	180												
		OL = 13 pr , b = VCCB		1.8–2.8	1.8–2.8	ı	49.6	150	-	150												
			EN/EN	1.8–3.6	1.8–3.6	ı	42.5	100	-	100												
			to A	0.9–3.6	0.9–3.6	ı	113.4	300	_	300												
		C _L = 15 pF; B = 0 V		1.2–1.8	1.2–1.8	-	100	250	-	250	ns											
		СL = 15 рг, в = 0 V		1.8–2.8	1.8–2.8	-	94.3	200	-	200	115											
	Outsut Enable Time			1.8–3.6	1.8–3.6	-	90.9	170	-	170												
t _{EN}	Output Enable Time	the street that the street Lagrangian C_L is perfectly a superficient C_L in the street C_L in the street C_L is perfectly C_L in the street C_L in the s		0.9–3.6	0.9–3.6	-	116.3	200	-	200												
				1.2–1.8	1.2–1.8	-	64.5	180	-	180												
				1.8–2.8	1.8–2.8	_	49.6	150	_	150												
			EN/EN	1.8–3.6	1.8–3.6	-	42.5	100	_	100												
			to B	0.9–3.6	0.9–3.6	_	113.4	300	_	300												
			C _L = 15 pF; A = 0 V		1.2–1.8	1.2–1.8	_	100	250	_	250											
					1.8-2.8	1.8-2.8	-	94.3	200	-	200	ns										
				1.8–3.6	1.8–3.6	_	90.9	170	_	170												
				0.9-3.6	0.9-3.6	-	255	600	_	600												
		O 45 . E D . V		1.2–1.8	1.2–1.8	-	180	350	_	350												
		$C_L = 15 pF; B = V_{CCB}$	$C_L = 15 \text{ pF}; B = V_{CCB}$	$C_L = 15 \text{ pF}; B = V_{CCB}$	$C_L = 15 \text{ pH}; B = V_{CCB}$	U _L = 15 pF; B = V _{CCB}	$C_L = 15 \text{ pF}; B = V_{CCB}$	$C_L = 15 \text{ pF}; B = V_{CCB}$		1.8–2.8	1.8–2.8	-	166.7	350	-	350						
			EN/EN	1.8–3.6	1.8–3.6	_	155.6	300	_	300												
			to A	0.9–3.6	0.9-3.6	-	156.7	400	_	400												
		0 45 E B 014		1.2–1.8	1.2-1.8	-	140	300	-	300												
		C _L = 15 pF; B = 0 V		1.8–2.8	1.8–2.8	-	130.2	300	-	300												
	O to I Disable Time			1.8-3.6	1.8-3.6	-	124.6	250	-	250												
t _{DIS}	Output Disable Time			0.9–3.6	0.9-3.6	-	255	600	-	600	ns											
		0 45 =5: 4 1/		1.2–1.8	1.2–1.8	-	180	350	-	350												
	$C_L = 15 \text{ pF; A} = V_{CCA}$	OL = 15 pr; A = V _{CCA}		1.8–2.8	1.8–2.8	-	166.7	350	-	350												
		EN/EN	1.8–3.6	1.8–3.6	-	155.6	300	-	300													
			t	to B	0.9–3.6	0.9-3.6	-	156.7	400	-	400											
						C _L = 15 pF; A = 0 V									1.2–1.8	1.2–1.8	-	140	300	_	300	1
															1.8–2.8	1.8–2.8	-	130.2	300	-	300	
				1.8–3.6	1.8–3.6	İ	124.6	250	-	250												

^{3.} Typical values are for $T_A = +25^{\circ}C$. Limits over the operating temperature range are guaranteed by design. 4. Guaranteed by design.

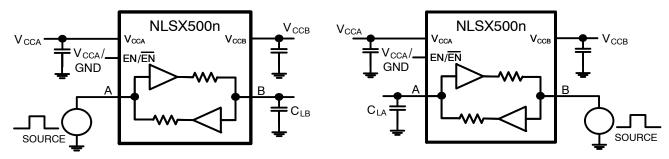


Figure 8. Driving A-Port Test Circuit (t_{PD})

Figure 9. Driving B-Port Test Circuit (t_{PD})

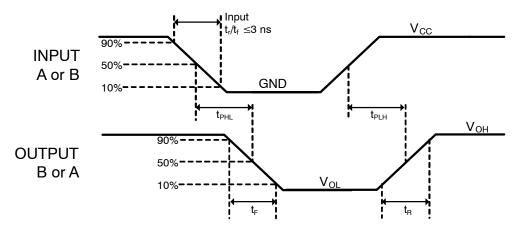


Figure 10. t_{PD} (t_{PLH}/t_{PHL}) Propagation Delay Measurements

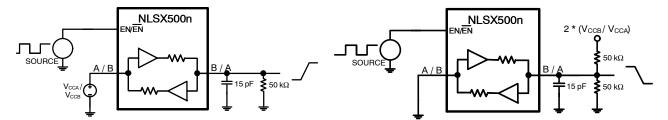


Figure 11. Enable/Disable Test Circuit (t_{PZH}/t_{PHZ})

Figure 12. Enable/Disable Test Circuit (t_{PZL}/t_{PLZ})

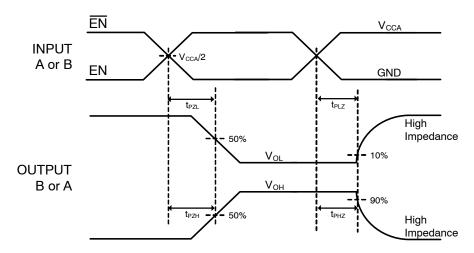


Figure 13. $t_{\text{EN}}/t_{\text{DIS}}$ $(t_{\text{PZL}}/t_{\text{PLZ}}/t_{\text{PZH}}/t_{\text{PHZ}})$ Propagation Delay Measurements

IMPORTANT APPLICATIONS INFORMATION

Level Translator Architecture

The NLSX5004 and the NLSXN5004 auto-sense translators provide bi-directional logic voltage level shifting to transfer data in multiple supply voltage systems. These level translators have two supply voltages, $V_{\rm CCA}$ and $V_{\rm CCB}$, which set the logic levels on the input and output sides of the translator. When used to transfer data from the A to the B ports, input signals referenced to the $V_{\rm CCA}$ supply are translated to output signals with a logic level matched to $V_{\rm CCB}$. In a similar manner, the B to A translation shifts input signals with a logic level compatible to $V_{\rm CCB}$ to an output signal matched to $V_{\rm CCA}$.

The NLSX5004 and the NLSXN5004 translators consist of bi-directional channels that independently determine the direction of the data flow without requiring a directional pin. One-shot circuits are used to detect the rising or falling input signals. In addition, the one-shots decrease the rise and fall times of the output signal for high-to-low and low-to-high transitions.

Input Driver Requirements

The NLSX5004 and NLSXN5004 support high data rates, but these translators have relatively modest DC output current drive. The high data rate of the bi-directional I/O circuit is used to quickly transform from an input to an output driver and vice versa. Each I/O port has a modest DC current output so that the internal output driver can be over-driven when data is sent in the opposite direction. For proper operation, the input driver to the auto-sense translator should be capable of driving 5.0 mA of peak output current. The bi-directional configuration of the translator results in both input stages being active for a very short time period. Although the peak current required from the input signal circuit is relatively large, the average current is small and consistent with a standard CMOS input stage.

Enable Input (EN/EN)

The NLSX5004 and NLSXN5004 translators have enable pins that provide tri-state operation at the I/O ports.

Driving the NLSX5004 Enable pin (EN) to a low logic level minimizes the power consumption of the device and drives the A- and B-ports to high impedance states. Normal translation operation occurs when the EN pin is equal to a logic high signal.

Driving NLSXN5004 Enable pin (\overline{EN}) to a high logic level minimizes the power consumption of the device and drives the A– and B–ports to high impedance states. Normal translation operation occurs when the \overline{EN} pin is equal to a logic low signal.

Both EN and \overline{EN} pins are referenced to the V_{CCA} supply and are Over-Voltage Tolerant (OVT).

Uni-Directional versus Bi-Directional Translation

The NLSX5004 and NLSXN5004 translators can function as non-inverting uni-directional translators. One advantage of using these translators as uni-directional devices is that each I/O-port can be configured as either an input or an output. The configurable input or output feature is especially useful in applications such as SPI that use multiple uni-directional I/O lines to send data to and from a device. The flexible I/O port of the auto sense translator simplifies the trace connections on the PCB.

Power Supply Guidelines

The values of the V_{CCA} and V_{CCB} supplies can be set to anywhere between 0.9 and 3.6 V. Design flexibility is maximized because V_{CCA} may be either greater than, equal to or less than the V_{CCB} supply.

The sequencing of the power supplies will not damage the device during power–up operation. In addition, the A– and B–ports are in high impedance states if either supply voltage is equal to 0 V. For optimal performance, 0.01 to 0.1 μ F decoupling capacitors should be used on the V_{CCA} and V_{CCB} power supply pins. Ceramic capacitors are a good design choice to filter and bypass any noise signals on the voltage lines to the ground plane of the PCB. The noise immunity will be maximized by placing the capacitors as close as possible to the supply and ground pins, along with minimizing the PCB connection traces.

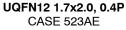
DEVICE ORDERING INFORMATION

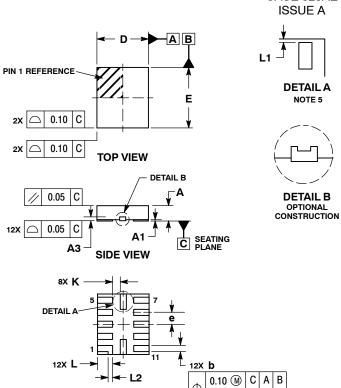
Device Order Number	Package Type	Tape & Reel Size [†]
NLSX5004MUTAG	UQFN-12	3000 Units/Reel
NLVSX5004MUTAG*	UQFN-12	3000 Units/Reel
NLSX5004DR2G (In Development)	SOIC14	2500 Units/Reel
NLVSX5004DR2G* (In Development)	SOIC14	2500 Units/Reel
NLSX5004DTR2G (In Development)	TSSOP14	2500 Units/Reel
NLVSX5004DTR2G* (In Development)	TSSOP14	2500 Units/Reel
NLSX5004MN1TXG (In Development)	QFN14, 3.5 x 3.5 x 0.5P	3000 Units/Reel
NLVSX5004MN1TXG*	QFN14, 3.5 x 3.5 x 0.5P	3000 Units/Reel
NLSX5004MN1TWG (In Development)	QFN14, 2.5 x 3.0 x 0.5P	3000 Units/Reel
NLVSX5004MN1TWG* (In Development)	QFN14, 2.5 x 3.0 x 0.5P	3000 Units/Reel
NLSXN5004MU2TAG (In Development)	UQFN-12	3000 Units/Reel
NLVSXN5004MU2TAG* (In Development)	UQFN-12	3000 Units/Reel
NLSXN5004DR2G (In Development)	SOIC14	2500 Units/Reel
NLVSXN5004DR2G* (In Development)	SOIC14	2500 Units/Reel
NLSXN5004DTR2G (In Development)	TSSOP14	2500 Units/Reel
NLVSXN5004DTR2G* (In Development)	TSSOP14	2500 Units/Reel
NLSXN5004MN1TXG (In Development)	QFN14, 3.5 x 3.5 x 0.5P	3000 Units/Reel
NLVSXN5004MN1TXG* (In Development)	QFN14, 3.5 x 3.5 x 0.5P	3000 Units/Reel
NLSXN5004MN1TWG (In Development)	QFN14, 2.5 x 3.0 x 0.5P	3000 Units/Reel
NLVSXN5004MN1TWG* (In Development)	QFN14, 2.5 x 3.0 x 0.5P	3000 Units/Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

^{*}NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable

PACKAGE DIMENSIONS





0.05 M

C NOTE 3

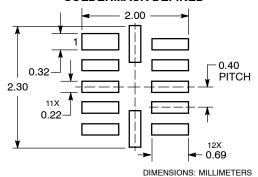
BOTTOM VIEW

NOTES:

- VOIES:
 1. DIMENSIONING AND TOLERANCING PER ASME
 Y14.5M, 1994.
 2. CONTROLLING DIMENSION: MILLIMETERS
 3. DIMENSION & APPLIES TO PLATED TERMINAL
 AND IS MEASURED BETWEEN 0.15 AND 0.30 MM
- FROM TERMINAL TIP.
 MOLD FLASH ALLOWED ON TERMINALS
 ALONG EDGE OF PACKAGE. FLASH 0.03
 MAX ON BOTTOM SURFACE OF
- TERMINALS.
 5. DETAIL A SHOWS OPTIONAL CONSTRUCTION FOR TERMINALS.

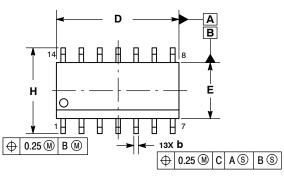
		MILLIN	IETERS
	DIM	MIN	MAX
	Α	0.45	0.55
	A1	0.00	0.05
	A3	0.127	REF
	b	0.15	0.25
	D	1.70	BSC
Γ	Е	2.00	BSC
	е	0.40	BSC
	K	0.20	
	L	0.45	0.55
	L1	0.00	0.03
Γ	L2	0.15	REF

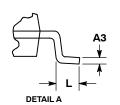
MOUNTING FOOTPRINT SOLDERMASK DEFINED

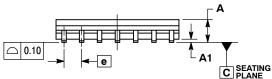


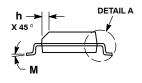
PACKAGE DIMENSIONS

SOIC-14 NB CASE 751A-03 **ISSUE L**









- NOTES:

 1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.

 2. CONTROLLING DIMENSION: MILLIMETERS.

 3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF AT MAXIMUM MATERIAL CONDITION.

 4. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSIONS.

 5. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.

	MILLIN	IETERS	INCHES		
DIM	MIN	MAX	MIN	MAX	
Α	1.35	1.75	0.054	0.068	
A1	0.10	0.25	0.004	0.010	
А3	0.19	0.25	0.008	0.010	
b	0.35	0.49	0.014	0.019	
D	8.55	8.75	0.337	0.344	
Е	3.80	4.00	0.150	0.157	
е	1.27	BSC	0.050	BSC	
Н	5.80	6.20	0.228	0.244	
h	0.25	0.50	0.010	0.019	
L	0.40	1.25	0.016	0.049	
М	0 °	7 °	0 °	7°	

SOLDERING FOOTPRINT* 6.50 14X 1.18 1.27 PITCH 14X 0.58

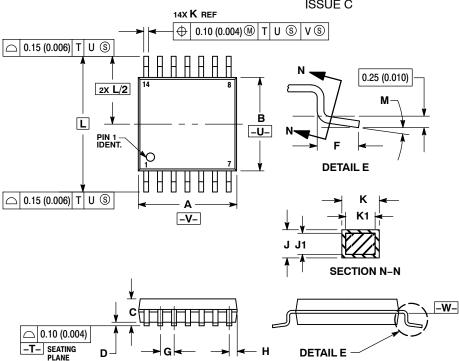
DIMENSIONS: MILLIMETERS

^{*}For additional information on our Pb–Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PACKAGE DIMENSIONS

TSSOP-14 WB

CASE 948G **ISSUE C**



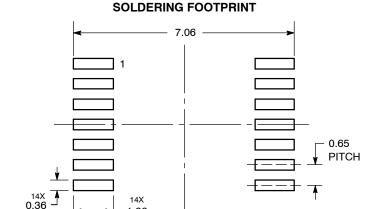
NOTES:

- 1. DIMENSIONING AND TOLERANCING PER
- ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: MILLIMETER.
 3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
- FLASH, PROTRUSIONS OR GATE BURRS.
 MOLD FLASH OR GATE BURRS SHALL NOT
 EXCEED 0.15 (0.006) PER SIDE.

 DIMENSION B DOES NOT INCLUDE
 INTERLEAD FLASH OR PROTRUSION.
 INTERLEAD FLASH OR PROTRUSION SHALL
 NOT EXCEED 0.25 (0.010) PER SIDE.

 DIMENSION K DOES NOT INCLUDE DAMBAR
 PROTRUSION. ALLOWABLE DAMBAR
 PROTRUSION. SHALL BE 0.08 (0.003) TOTAL
 IN EXCESS OF THE K DIMENSION AT
 MAXIMUM MATERIAL CONDITION.
 TERMINAL NUMBERS ARE SHOWN FOR
- TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
 DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

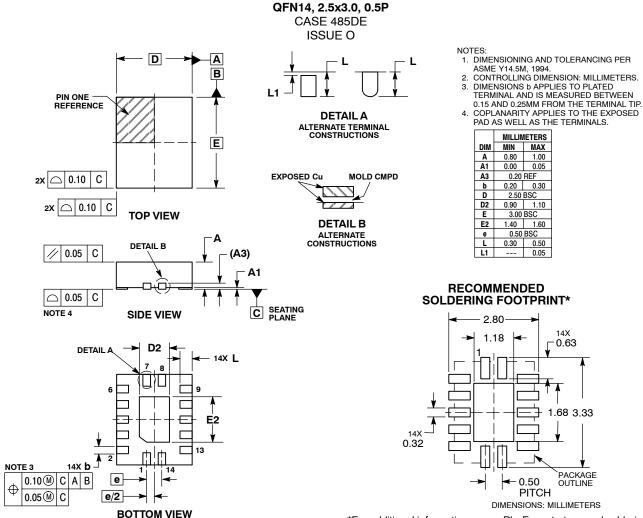
	MILLIN	IETERS	INCHES			
DIM	MIN	MAX	MIN	MAX		
Α	4.90	5.10	0.193	0.200		
В	4.30	4.50	0.169	0.177		
С		1.20		0.047		
D	0.05	0.15	0.002	0.006		
F	0.50	0.75	0.020	0.030		
G	0.65	BSC	0.026 BSC			
Н	0.50	0.60	0.020	0.024		
J	0.09	0.20	0.004	0.008		
J1	0.09	0.16	0.004	0.006		
Κ	0.19	0.30	0.007	0.012		
K1	0.19	0.25	0.007	0.010		
L	6.40	BSC	0.252	BSC		
М	0 °	8 °	0 °	8 °		



DIMENSIONS: MILLIMETERS

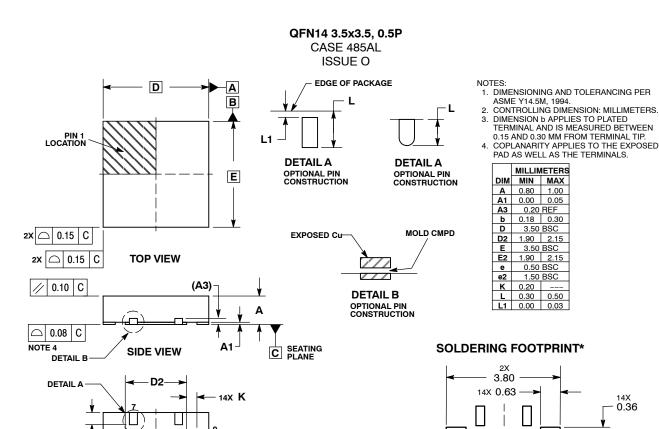
14X 1.26

PACKAGE DIMENSIONS



^{*}For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PACKAGE DIMENSIONS



E2

0.05 С NOTE 3

0.10 C A B

14X b

Ф

DIMENSIONS: MILLIMETERS

- 1.50 PITCH

0.50 **PITCH**

14X 0.36

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

2X 2.12

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