**Product data sheet** 

## 1. Product profile

## 1.1 General description

Passivated sensitive gate Silicon-Controlled Rectifier (SCR) in a SOT54 plastic package

### 1.2 Features

- Direct interfacing to logic level ICs
- Direct interfacing to low-power gate drive circuits
- For operation on DC and rectified AC supplies

## 1.3 Applications

- Christmas lights control
- Protection and safety shutdown circuits e.g. lighting ballasts

### 1.4 Quick reference data

- $V_{DRM} \leq 400 \text{ V}$
- $I_{TSM} \le 8 \text{ A (t = 10 ms)}$
- $I_{T(RMS)} \le 0.8 A$
- $I_{T(AV)} \le 0.5 A$

## 2. Pinning information

Table 1. Pinning

Pin	Description	Simplified outline	Graphic symbol
1	anode (A)		
2	gate (G)		A H
3	cathode (K)		G sym037
		SOT54 (TO-92)	



**SCR logic level** 

# 3. Ordering information

## Table 2. Ordering information

Type number	Package	Package				
	Name	Description	Version			
NXL0840	TO-92	plastic single-ended leaded (through hole) package; 3 leads	SOT54			

# 4. Limiting values

## Table 3. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Parameter	Conditions	Min	Max	Unit
repetitive peak off-state voltage		-	400	V
average on-state current	half sine wave; $T_{lead} \le 83 ^{\circ}\text{C}$ ; see Figure 1	-	0.5	Α
RMS on-state current	all conduction angles; see <u>Figure 4</u> and <u>5</u>	-	0.8	Α
non-repetitive peak on-state current	half sine wave; $T_j = 25$ °C prior to surge; see Figure 2 and 3			
	t = 10 ms	-	8	А
	t = 8.3 ms	-	9	Α
I <sup>2</sup> t for fusing	t <sub>p</sub> = 10 ms	-	0.32	A <sup>2</sup> s
rate of rise of on-state current	$I_{TM} = 2 \text{ A}; I_G = 10 \text{ mA};$ $dI_G/dt = 100 \text{ mA}/\mu\text{s}$	-	50	A/μs
peak gate current		-	1	А
peak gate voltage		-	5	V
peak reverse gate voltage		-	5	V
peak gate power		-	2	W
average gate power	over any 20 ms period	-	0.1	W
storage temperature		-40	+150	°C
junction temperature		-	125	°C
	repetitive peak off-state voltage average on-state current  RMS on-state current  non-repetitive peak on-state current  I²t for fusing rate of rise of on-state current  peak gate current peak gate voltage peak reverse gate voltage peak gate power average gate power storage temperature	repetitive peak off-state voltage	repetitive peak off-state voltage average on-state current half sine wave; $T_{lead} \le 83  ^{\circ}\text{C}$ ; see Figure 1 all conduction angles; see Figure 4 and 5 half sine wave; $T_j = 25  ^{\circ}\text{C}$ prior to surge; see Figure 2 and 3	repetitive peak off-state voltage $-400$ average on-state current half sine wave; $T_{lead} \le 83  ^{\circ}\text{C}$ ; $-30.5$ see Figure 1 all conduction angles; see Figure 4 and 5 half sine wave; $T_j = 25  ^{\circ}\text{C}$ prior to surge; see Figure 2 and 3 $-30.32  ^{\circ}$ to $-30.32  ^{\circ$

**SCR logic level** 

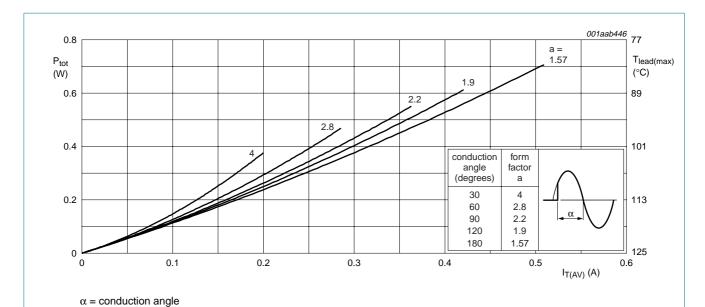


Fig 1. Total power dissipation as a function of average on-state current; maximum values

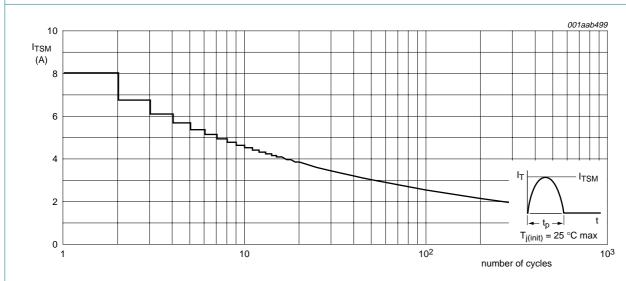


Fig 2. Non-repetitive peak on-state current as a function of the number of sinusoidal current cycles; maximum values

f = 50 Hz

**SCR logic level** 

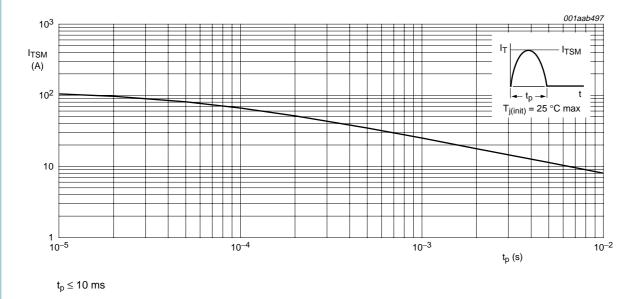


Fig 3. Non-repetitive peak on-state current as a function of pulse width; maximum values

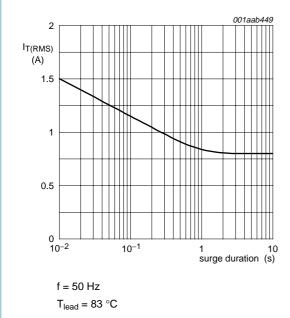


Fig 4. RMS on-state current as a function of surge duration; maximum values

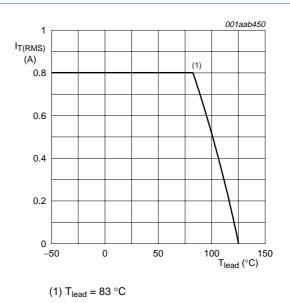


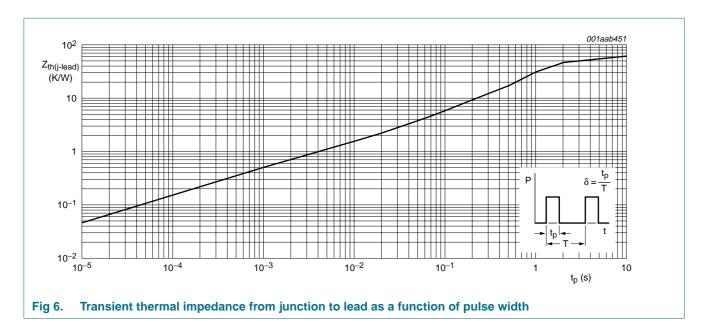
Fig 5. RMS on-state current as a function of lead temperature; maximum values

**SCR logic level** 

## 5. Thermal characteristics

Table 4. Thermal characteristics

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
$R_{th(j\text{-lead})}$	thermal resistance from junction to lead	see Figure 6	-	-	60	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	printed circuit board mounted; lead length 4 mm	-	150	-	K/W



**SCR logic level** 

## 6. Characteristics

Table 5. Characteristics

 $T_i = 25 \,^{\circ}C$  unless otherwise specified.

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
Static ch	naracteristics		'	'	· ·	'
I <sub>GT</sub>	gate trigger current	$V_D = 12 \text{ V}; I_T = 10 \text{ mA}; \text{see } \frac{\text{Figure 8}}{\text{M}}$	-	50	200	μΑ
IL	latching current	$V_D$ = 12 V; $I_G$ = 0.5 mA; $R_{GK}$ = 1 k $\Omega$ ; see Figure 10	-	2	6	mA
I <sub>H</sub>	holding current	$V_D$ = 12 V; $I_G$ = 0.5 mA; $R_{GK}$ = 1 k $\Omega$ ; see Figure 11	-	2	5	mA
$V_{T}$	on-state voltage	I <sub>T</sub> = 1.2 A; see <u>Figure 9</u>	-	1.25	1.7	V
V <sub>GT</sub> gate trigger voltage		I <sub>T</sub> = 10 mA; see <u>Figure 7</u>				
		V <sub>D</sub> = 12 V	-	0.5	0.8	V
		$V_D = V_{DRM(max)}$ ; $T_j = 125  ^{\circ}C$	0.2	0.3	-	V
I <sub>D</sub>	off-state current	$V_D = V_{DRM(max)}$ ; $T_j = 125$ °C; $R_{GK} = 1 \text{ k}\Omega$	-	0.05	0.1	mΑ
Dynamic	c characteristics					
dV <sub>D</sub> /dt	rate of rise of off-state voltage	$V_{DM}$ = 0.67 × $V_{DRM(max)}$ ; $T_j$ = 125 °C; exponential waveform; see Figure 12				
		$R_{GK} = 1 k\Omega$	200	600	-	V/μs
		gate open circuit	-	25		V/μs

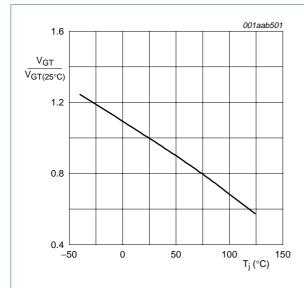


Fig 7. Normalized gate trigger voltage as a function of junction temperature

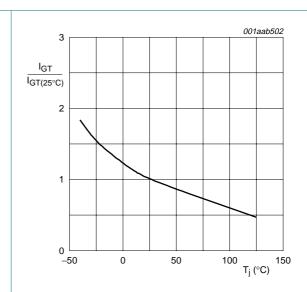


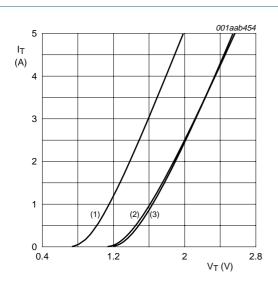
Fig 8. Normalized gate trigger current as a function of junction temperature

NXL0840\_1 © NXP B.V. 2008. All rights reserved.

**NXL0840 NXP Semiconductors** 

**SCR logic level** 

100 T<sub>j</sub> (°C)



 $V_0 = 1.067 \text{ V}$ 

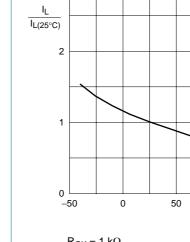
 $R_s = 0.187 \Omega$ 

(1)  $T_i = 125$  °C; typical values

(2)  $T_i = 125 \,^{\circ}C$ ; maximum values

(3)  $T_j = 25$  °C; maximum values

On-state current as a function of on-state Fig 9. voltage



3

 $R_{GK} = 1 k\Omega$ 

Fig 10. Normalized latching current as a function of junction temperature

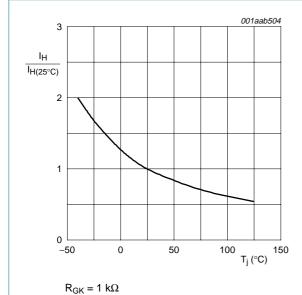
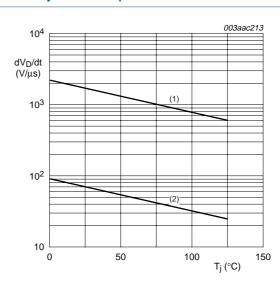


Fig 11. Normalized holding current as a function of junction temperature



(1)  $R_{GK} = 1 k\Omega$ 

(2) Gate open-circuit

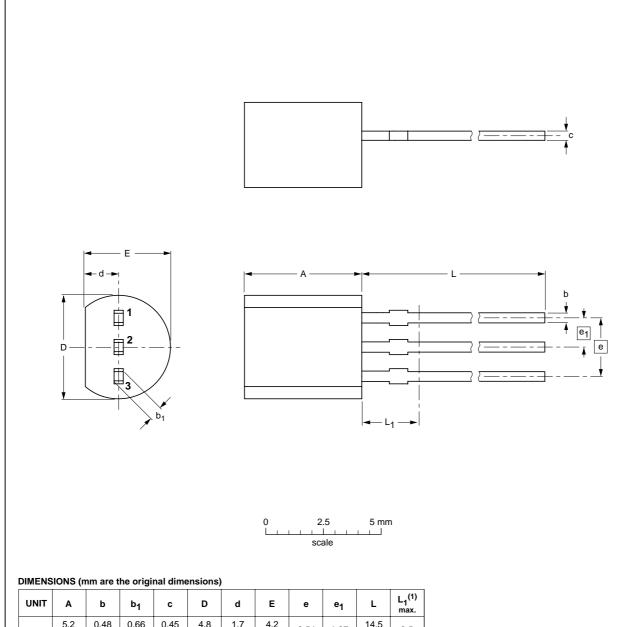
Fig 12. Critical rate of rise of off-state voltage as a function of junction temperature; typical values

NXL0840\_1 © NXP B.V. 2008. All rights reserved.

# **Package outline**

# Plastic single-ended leaded (through hole) package; 3 leads

SOT54



UNIT	А	b	b <sub>1</sub>	С	D	d	E	е	e <sub>1</sub>	L	L <sub>1</sub> <sup>(1)</sup> max.
mm	5.2 5.0	0.48 0.40	0.66 0.55	0.45 0.38	4.8 4.4	1.7 1.4	4.2 3.6	2.54	1.27	14.5 12.7	2.5

1. Terminal dimensions within this zone are uncontrolled to allow for flow of plastic and terminal irregularities.

OUTLINE			REFERENCES				ISSUE DATE	
	VERSION	IEC	JEDEC	JEDEC JEITA PROJEC		PROJECTION	ISSUE DATE	
	SOT54		TO-92	SC-43A			<del>04-06-28</del> 04-11-16	

Fig 13. Package outline SOT54 (TO-92)

SCR logic level

9 of 11

# 8. Revision history

## Table 6. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
NXL0840_1	20080226	Product data sheet	-	-

SCR logic level

## 9. Legal information

### 9.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions"
- [3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

### 9.2 Definitions

Draft — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

Short data sheet — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

## 9.3 Disclaimers

**General** — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in medical, military, aircraft, space or life support equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental

damage. NXP Semiconductors accepts no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

**Applications** — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Limiting values — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) may cause permanent damage to the device. Limiting values are stress ratings only and operation of the device at these or any other conditions above those given in the Characteristics sections of this document is not implied. Exposure to limiting values for extended periods may affect device reliability.

Terms and conditions of sale — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at <a href="http://www.nxp.com/profile/terms">http://www.nxp.com/profile/terms</a>, including those pertaining to warranty, intellectual property rights infringement and limitation of liability, unless explicitly otherwise agreed to in writing by NXP Semiconductors. In case of any inconsistency or conflict between information in this document and such terms and conditions, the latter will prevail.

**No offer to sell or license** — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

**Quick reference data** — The Quick reference data is an extract of the product data given in the Limiting values and Characteristics sections of this document, and as such is not complete, exhaustive or legally binding.

### 9.4 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

### 10. Contact information

For more information, please visit: http://www.nxp.com

For sales office addresses, please send an email to: salesaddresses@nxp.com

NXL0840\_1 © NXP B.V. 2008. All rights reserved.

**NXP Semiconductors** 

# **NXL0840**

## **SCR logic level**

## 11. Contents

1	Product profile
1.1	General description
1.2	Features
1.3	Applications
1.4	Quick reference data
2	Pinning information 1
3	Ordering information 2
4	Limiting values 2
5	Thermal characteristics 5
6	Characteristics 6
7	Package outline 8
8	Revision history 9
9	Legal information 10
9.1	Data sheet status
9.2	Definitions
9.3	Disclaimers
9.4	Trademarks
10	Contact information 10
11	Contents

Please be aware that important notices concerning this document and the product(s) described herein, have been included in section 'Legal information'.

