

#### MAIA-011004

Rev. V3

#### Features

- 2-Stage LNA and High Power Switch
  - High RF Input Power: 120 W CW @ +85°C, 2.0 GHz 100 W CW @ +85°C, 2.7 GHz
- Noise Figure: 0.85 dB @ 2.0 GHz 1.0 dB @ 2.7 GHz
- Gain:
  - 37 dB @ 2.0 GHz 34 dB @ 2.7 GHz
- OIP3: 36 dBm
- Lead-Free 5 mm 32-lead HQFN
- Integrated ESD Protection
- Halogen-Free "Green" Mold Compound
- ROHS\* Compliant

#### Description

The MAIA-011004 is a compact surface mount module containing a PIN diode switch and two low noise amplifiers assembled in a 5 mm 32-lead HQFN plastic package. It was designed to be used at the input of the receive chain of TDD cellular base stations.

This module operates from 0.4 GHz to 5.0 GHz and features high power handling, very low noise figure and excellent linearity.

The connection between the output of LNA1 and the input of LNA2 is made outside of the module, making it possible for the user to add an attenuator or a filter.

The MAIA-011004 is ideally suited for 4G and next generation 5G base stations at 1.9, 2.3, 2.6, 3.5, and 4.5 GHz.

#### **Ordering Information**<sup>1,2</sup>

Part Number	Package
MAIA-011004-TR1000	1k Piece Reel
MAIA-011004-TR3000	3k Piece Reel
MAIA-011004-1SMB	2 - 3 GHz Sample Board
MAIA-011004-2SMB	3 - 4 GHz Sample Board

1. Reference Application Note M513 for reel size information.

2. All sample boards include 5 loose parts.

\* Restrictions on Hazardous Substances, compliant to current RoHS EU directive.



#### Pin Configuration

Pin #	Pin Name	Function	
1-4, 6-10,12 16,18,23,25,32	N/C <sup>3</sup>	No Connection	
5	RF <sub>IN</sub>	RF Input / Bias	
11	R <sub>x</sub>	R <sub>X</sub> Switch Output	
13,14,20,21, 27,29,30	GND	RF Ground	
15	LNA1 <sub>IN</sub>	LNA1 Input	
17	V <sub>B</sub> 1	LNA1 Bias	
19	LNA1 <sub>OUT</sub>	LNA1 Output / V <sub>DD</sub> 1	
22	LNA2 <sub>IN</sub>	LNA2 Input	
24	RF <sub>OUT</sub>	RF Output / V <sub>DD</sub> 2	
26	V <sub>B</sub> 2	LNA2 Bias	
28	Vc	Switch Bias Control	
31	Load	T <sub>X</sub> Switch Output	
33	Paddle	Ground⁴	

3. MACOM recommends connecting unused package pins (N/C) to ground.

4. The exposed pad centered on the package bottom must be connected to RF, DC and thermal ground.

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#### Electrical Specifications<sup>5</sup>:

#### $T_A$ = +25°C, $V_{DD}$ 1 = 3 V, $V_{BB}$ 1 = 3 V, $V_{DD}$ 2 = 3 V, $V_{BB}$ 2 = 3 V Switch Bias = (see Bias Table), $R_{BIAS}$ 2 = 133 Ω, $R_{BIAS}$ 1 = 100 Ω, $Z_0$ = 50 Ω

Parameter	Test Conditions	Units	Min.	Тур.	Max.
Input RF Power @ +85°C RF <sub>IN</sub> - LOAD	2.0 GHz 2.7 GHz 3.5 GHz	W	_	120 100 80	_
Insertion Loss RF <sub>IN</sub> - LOAD	2.0 GHz 2.7 GHz 3.5 GHz	dB	_	0.15 0.18 0.21	_
Noise Figure RF <sub>IN -</sub> RF <sub>OUT</sub>	2.0 GHz 2.7 GHz 3.5 GHz	dB		0.85 1.00 1.25	
Gain RF <sub>IN -</sub> RF <sub>OUT</sub>	2.0 GHz 2.7 GHz 3.5 GHz	dB	_	37 34 32	
Isolation RF <sub>IN</sub> - LNA1 <sub>IN</sub>	Switch State = RF <sub>IN</sub> - LOAD 2.7 GHz	dB	—	41	_
Isolation LNA1 <sub>OUT</sub> - LNA2 <sub>IN</sub>	Switch State = RF <sub>IN</sub> - RF <sub>OUT</sub> 2.7 GHz	dB	_	40	_
Output IP3 RF <sub>IN -</sub> RF <sub>OUT</sub>	P <sub>IN</sub> = -35 dBm, Tones 11 MHz apart 2.7 GHz	dBm	_	36	—
LNA Bias Current	LNA1 Current: $I_{DD}1 + IV_B1$ LNA2 Current: $I_{DD}2 + IV_B2$	mA	_	75 65	_

5. Refer to LNA biasing options on page 4.

#### Switch Bias Table (See Sample Board Schematic on Page 9)

RF <sub>IN</sub> – LOAD	RF <sub>IN</sub> – RF <sub>OUT</sub>	LOAD_B	<b>R</b> <sub>x</sub> Bias	Rx_ShD_B	V_RF <sub>IN</sub>
ON	OFF	0 V (-50 mA)	+28 V (50 mA)	0 V (-50 mA)	3 V (50 mA)
OFF	ON	+28 V (0 mA)	0 V (-50 mA)	+28 V (0 mA)	3 V (50 mA)

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#### Absolute Maximum Ratings<sup>6,7,8</sup>

Parameter	Absolute Maximum
RF Input Power RF <sub>IN -</sub> RF <sub>OUT</sub> RF <sub>IN</sub> - LOAD	19 dBm See Power De-rating Curve
Switch Reverse Voltage (RF & DC)	160 V
V <sub>B</sub> 1 & V <sub>B</sub> 2	5.0 V
LNA1 <sub>OUT</sub> & RF <sub>OUT</sub>	5.5 V
Junction Temperature Switch LNA <sup>9</sup>	+175°C +150°C
Operating Temperature	-40°C to +100°C
Storage Temperature	-55°C to +150°C

6. Exceeding any one or combination of these limits may cause permanent damage to this device.

- MACOM does not recommend sustained operation near these survivability limits.
- 8. Operating at nominal conditions with  $T_J \le$  Absolute Maximum will ensure MTTF >1 x 10<sup>6</sup> hours.
- 9. LNA Junction Temperature (T<sub>J</sub>) = T<sub>C</sub> +  $\Theta_{JC}^*$ (V\*I) Typical thermal resistance ( $\Theta_{JC}$ ) = 83°C/W
  - a) For  $T_c = +25^{\circ}C$ ,  $T_J = 56^{\circ}C @ V_{DD}1 = 5 V$ , 75 mA for LNA1  $T_J = 52^{\circ}C @ V_{DD}2 = 5 V$ , 65 mA for LNA2
  - b) For  $T_c = +100 \ ^\circ C$ ,
    - $T_J = 131^{\circ}C @ V_{DD}1 = 5 V, 75 mA for LNA1$  $T_J = 127^{\circ}C @ V_{DD}1 = 5 V, 65 mA for LNA2$

#### T<sub>x</sub> Input Power De-rating @ 20 dB I/O Return Loss



#### Handling Procedures

Please observe the following precautions to avoid damage:

#### Static Sensitivity

These electronic devices are sensitive to electrostatic discharge (ESD) and can be damaged by static electricity. Proper ESD control techniques should be used when handling these devices.

Parameter	Rating	Standard
Human Body Model	500 V	ESDA / JEDEC
(HBM)	(Class 1B)	JS-001
Charged Device	1000 V	JEDEC
Model (CDM)	(Class C3)	JESD22-C101

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#### LNA Biasing Options

LNA1 and LNA2 biases can be set in 2 different ways: using only  $V_{DD}$ , or using separate  $V_{DD}$  and  $V_{BIAS}$  [V<sub>B</sub>] voltages. A separate  $V_{BIAS}$  voltage allows  $V_B1$  and  $V_B2$  to be used as enable pins to power LNA1 and LNA2 up and down during operation.

For both bias methods, select the value of  $R_{BIAS}1$  and  $R_{BIAS}2$  to achieve the desired currents using the plots on page 5. LNA1 current should not exceed 100 mA @ 25 °C and likewise LNA2 current should not exceed 95 mA @ 25 °C. DC blocking capacitors must be used at the LNA1 and 2 input and output ports (see diagram).

#### Biasing Option - V<sub>DD</sub> only

To use only  $V_{DD}$ , connect to  $V_{DD}$  [1,2] through an RF inductor and connect  $V_B$  [1,2] to the corresponding  $V_{DD}$  through bias resistor  $R_{BIAS}$  [1,2] as shown in Figure 1.



Figure 1

#### Biasing Option - Separate $V_{DD}$ and $V_{BB}$ Voltages ( $V_{BB} \leq V_{DD}$ )

To use separate  $V_{DD}$  and  $V_{BB}$  voltages, connect to  $V_{DD}$  [1,2] through an RF inductor and connect to  $V_{BB}$  [1,2] through bias resistor  $R_{BIAS}$  [1,2] as shown in Figure 2. Typical current draw for  $V_B$ [1,2] is 1.4 mA @  $V_{BB}$  = 3 V ,and 1  $\mu$ A @  $V_{BB}$  = 0 V. Typical current draw for  $V_{DD}$  [1,2] is < 1  $\mu$ A @  $V_{BB}$  = 0 V and  $V_{DD}$  = 3V.



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#### Typical Performance Curves: LNA1 Bias Current over Temperature

#### LNA1 Current, V<sub>DD</sub>1 = 3 V



#### Typical Performance Curves: LNA2 Bias Current over Temperature



#### LNA2 Current, V<sub>DD</sub>2 = 5 V

LNA1 Current, V<sub>DD</sub>1 = 5 V



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4

3V

5V

4

25 C

-40C

+85C

4

5

5

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Typical Performance Curves:  $T_A = +25^{\circ}C$ ,  $Z_0 = 50 \Omega$ ,  $V_{DD} = 3 V$ , Switch State = RF<sub>IN</sub> - RF<sub>OUT</sub>

6

20

0

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5

20

0

1

2

Frequency (GHz)

3

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1

2

3

Frequency (GHz)

4



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S11 vs. Switch Bias Current

S21 vs. Switch Bias Current







Isolation, RF<sub>IN</sub> to LNA1<sub>IN</sub> vs. Bias Current



S22 vs. Switch Bias Current



P1dB vs. Temperature, State = RF<sub>IN</sub> - RF<sub>OUT</sub>



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# Electrical Specifications: $T_A = +25^{\circ}C$ , $V_{DD}1 = 3 V$ , $V_{BB}1 = 3 V$ , $V_{DD}2 = 3 V$ , $V_{BB}2 = 3 V$ , Switch Bias = (see Bias Table), R5 = 133 $\Omega^{10}$ , R7 = 100 $\Omega^{10}$ ; Tuned for 2 - 3 GHz band

Parameter	Test Conditions	Units	Min.	Тур.	Max.
Gain	RF <sub>IN</sub> – RF <sub>OUT</sub> , 2.7GHz	dB	31	34	-
Noise Figure	RF <sub>IN</sub> – RF <sub>OUT</sub> , 2.7GHz	dB	_	1.1	1.5
Input Return Loss	RF <sub>IN</sub> – RF <sub>OUT</sub> , 2.7GHz	dB	_	11	-
Output Return Loss	RF <sub>IN</sub> – RF <sub>OUT</sub> , 2.7GHz	dB	_	18	_
LNA Bias Current	LNA1 Current: I <sub>DD</sub> 1 + IV <sub>B</sub> 1 LNA2 Current: I <sub>DD</sub> 2 + IV <sub>B</sub> 2	mA	_	75 65	—

10. Refer to LNA Sample Board Schematic on page 9.

### Typical Performance Curves: 2 - 3 GHz tuned Sample Board, RF<sub>IN</sub> - RF<sub>OUT</sub>



Noise Figure

**Output Return Loss** 







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3.0

+25C

+85C

2.8

-

2.6

2.4

Frequency (GHz)



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### Schematic: MAIA-011004 Sample Board



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#### PCB Layout: MAIA-011004 Sample Board J2 LOAD 83 **හ**( J1 ANT C5 U C12 Ç1 Σ 5 J3 RF OUT **C**14 ī e C15 📖 C6 R1 $V_RF_{IN}$ $\bigcirc$ 22

# Sample Board Parts List\* for 2 - 3 GHz Tuned PCB

Part	Value	Description	MFR Part #	
C1, C2, C5,	27 pF / 250 V	0603 SMT Capacitor	ATC600S270GT250T	
C3	22 pF / 250 V	0402 SMT Capacitor	ATC600L220FT200T	
C4	3.3 pF / 50 V	0402 SMT Capacitor	GRM1555C1H3R3BA01D	
C6, C7,C8, C9, C10, C13, C14, C15	4.7 µF / 35 V	0603 SMT Capacitor	_	
C11	10 nF / 25V	0402 SMT Capacitor	_	
C12	1 nF / 25V	0402 SMT Capacitor	—	
C21	0.40 pF ±0.1 pF	0402 SMT Capacitor	GJM1555C1HR40BB01	
L1, L2, L3, L5 ,L6, L9	68 nH / 100 mA	0402 SMT Inductor	0402CS-68NXJLW	
L4	2.7 nH	0402 SMT Inductor	0402CS-2N7XJLU	
L8	2.0 nH	0402 SMT Inductor	0402CS-2N0XJLU	
R1	45 Ω / 1.0 W	2512 SMT Resistor	—	
R3, R4	270 Ω / 1.0 W	2512 SMT Resistor	—	
R5 (R <sub>BIAS</sub> 2)	133 Ω	0805 SMT Resistor	—	
R7 (R <sub>BIAS</sub> 1)	100 Ω	0402 SMT Resistor	—	
J1 - J3	SMA END LAUNCH	RF CONNECTOR	142-0761-821	
R2, C16, C18, C19, C20, C22	R2, C16, C18, C19, C20, C22 do not populate			
	* Aluminum heat sink mounted	to backside of PCB is not show	n	

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Electrical Specifications:  $T_A = +25^{\circ}C$ ,  $V_{DD}1 = 3 V$ ,  $V_{BB}1 = 3 V$ ,  $V_{DD}2 = 3 V$ ,  $V_{BB}2 = 3 V$ , Switch Bias = (see Bias Table), R5 = 133  $\Omega^{10}$ , R7 = 100  $\Omega^{10}$ ; Tuned for 3 - 4 GHz band

Parameter	Test Conditions	Units	Min.	Тур.	Max.
Gain	RF <sub>IN</sub> – RF <sub>OUT</sub> , 3.5 GHz	dB	_	32	_
Noise Figure	RF <sub>IN</sub> − RF <sub>OUT</sub> , 3.5 GHz	dB	_	1.3	—
Input Return Loss	RF <sub>IN</sub> − RF <sub>OUT</sub> , 3.5 GHz	dB	_	12	—
Output Return Loss	RF <sub>IN</sub> − RF <sub>OUT</sub> , 3.5 GHz	dB	_	14	_
LNA Bias Current	LNA1 Current: I <sub>DD</sub> 1 + IV <sub>B</sub> 1 LNA2 Current: I <sub>DD</sub> 2 + IV <sub>B</sub> 2	mA	—	75 65	





Noise Figure

**Output Return Loss** 



Input Return Loss



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#### Sample Board Parts List\* for 3 - 4 GHz Tuned PCB

Part	Value	Description	MFR Part #		
C1, C2, C5	27 pF / 250 V	0603 SMT Capacitor	ATC600S270GT250T		
C3	22 pF / 250 V	0402 SMT Capacitor	ATC600L220FT200T		
C4, C12	1000 pF / 25 V	0402 SMT Capacitor	_		
C6, C7,C8, C9, C10, C13, C14, C15	4.7 µF / 35 V	0603 SMT Capacitor	_		
C11	10 nF / 25V	0402 SMT Capacitor	_		
C21	0.50 pF ±0.1 pF	0402 SMT Capacitor	GJM1555C1HR50BB01		
L1, L2, L3, L5 ,L6, L9	68 nH / 100 mA	0402 SMT Inductor	0402CS-68NXJLW		
L4	1.2 nH	0402 SMT Inductor	0402CS-1N2XJLU		
L8	2.0 nH	0402 SMT Inductor	0402CS-2N0XJLU		
R1	45 Ω / 1.0 W	2512 SMT Resistor	_		
R3, R4	270 Ω / 1.0 W	2512 SMT Resistor	_		
R5 (R <sub>BIAS</sub> 2)	133 Ω	0805 SMT Resistor	_		
R7 (R <sub>BIAS</sub> 1)	100 Ω	0402 SMT Resistor	_		
J1 - J3	SMA END LAUNCH	RF CONNECTOR	142-0761-821		
R2, C16, C18, C19, C20, C22	R2, C16, C18, C19, C20, C22 do not populate				
*,	Aluminum heat sink mounted	to backside of PCB is not show	n		

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#### Lead-Free 5 mm 32-Lead HQFN<sup>†</sup>



<sup>†</sup> Reference Application Note M538 for lead-free solder reflow recommendations. Meets JEDEC moisture sensitivity level 1 requirements. Plating is NiPdAuAg.

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