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MMBT6521LT1G, SMMBT6521LT1G

Amplifier Transistor

NPN Silicon

Features

- S Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q101 Qualified and PPAP Capable
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CEO}	25	Vdc
Collector–Base Voltage	V_{CBO}	40	Vdc
Emitter–Base Voltage	V_{EBO}	4.0	Vdc
Collector Current — Continuous	I_C	100	mAdc

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Total Device Dissipation FR–5 Board (Note 1) @ $T_A = 25^\circ\text{C}$ Derate above 25°C	P_D	225 1.8	mW mW/ $^\circ\text{C}$
Thermal Resistance, Junction–to–Ambient	$R_{\theta JA}$	556	$^\circ\text{C}/\text{W}$
Total Device Dissipation Alumina Substrate, (Note 2) @ $T_A = 25^\circ\text{C}$ Derate above 25°C	P_D	300 2.4	mW mW/ $^\circ\text{C}$
Thermal Resistance, Junction–to–Ambient	$R_{\theta JA}$	417	$^\circ\text{C}/\text{W}$
Junction and Storage Temperature	T_J, T_{stg}	–55 to +150	$^\circ\text{C}$

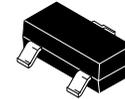
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. FR–5 = $1.0 \times 0.75 \times 0.062$ in.
2. Alumina = $0.4 \times 0.3 \times 0.024$ in. 99.5% alumina.

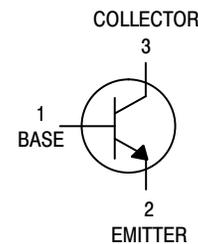


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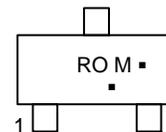
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SOT–23 (TO–236)
CASE 318–08
STYLE 6



MARKING DIAGRAM



RO = Specific Device Code
M = Date Code*
▪ = Pb-Free Package

(Note: Microdot may be in either location)

*Date Code orientation and/or overbar may vary depending upon manufacturing location.

ORDERING INFORMATION

Device	Package	Shipping†
MMBT6521LT1G	SOT–23 (Pb–Free)	3,000 / Tape & Reel
SMMBT6521LT1G	SOT–23 (Pb–Free)	3,000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

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ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector–Emitter Breakdown Voltage ($I_C = 0.5\text{ mAdc}$, $I_B = 0$)	$V_{(BR)CEO}$	25	–	Vdc
Emitter–Base Breakdown Voltage ($I_E = 10\text{ }\mu\text{Adc}$, $I_C = 0$)	$V_{(BR)EBO}$	4.0	–	Vdc
Collector Cutoff Current ($V_{CB} = 30\text{ Vdc}$, $I_E = 0$)	I_{CBO}	–	0.5	μAdc
Emitter Cutoff Current ($V_{EB} = 5.0\text{ Vdc}$, $I_C = 0$)	I_{EBO}	–	10	nAdc
ON CHARACTERISTICS				
DC Current Gain ($I_C = 100\text{ }\mu\text{Adc}$, $V_{CE} = 10\text{ Vdc}$) ($I_C = 2.0\text{ mAdc}$, $V_{CE} = 10\text{ Vdc}$)	h_{FE}	150 300	– 600	–
Collector–Emitter Saturation Voltage ($I_C = 50\text{ mAdc}$, $I_B = 5.0\text{ mAdc}$)	$V_{CE(sat)}$	–	0.5	Vdc
SMALL–SIGNAL CHARACTERISTICS				
Output Capacitance ($V_{CB} = 10\text{ Vdc}$, $I_E = 0$, $f = 1.0\text{ MHz}$)	C_{obo}	–	3.5	pF
Noise Figure ($I_C = 10\text{ }\mu\text{Adc}$, $V_{CE} = 5.0\text{ Vdc}$, Power Bandwidth = 15.7 kHz, 3.0 dB points @ = 10 Hz and 10 kHz)	NF	–	3.0	dB

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

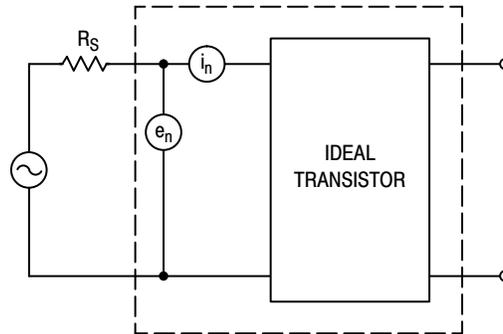


Figure 1. Transistor Noise Model

EQUIVALENT SWITCHING TIME TEST CIRCUITS

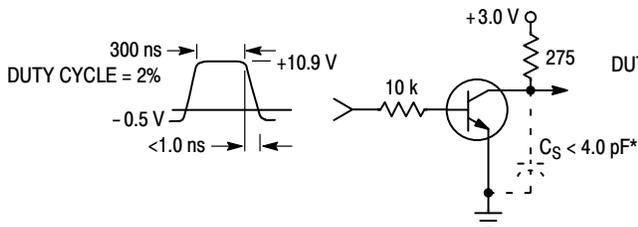


Figure 2. Turn-On Time

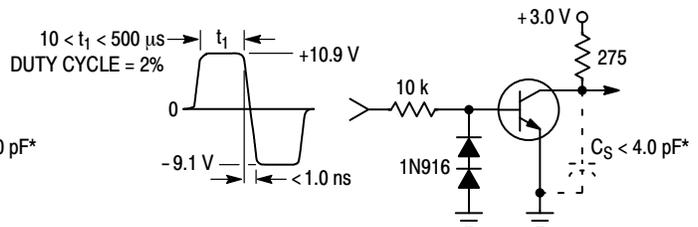


Figure 3. Turn-Off Time

*Total shunt capacitance of test jig and connectors

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TYPICAL NOISE CHARACTERISTICS

($V_{CE} = 5.0 \text{ Vdc}$, $T_A = 25^\circ\text{C}$)

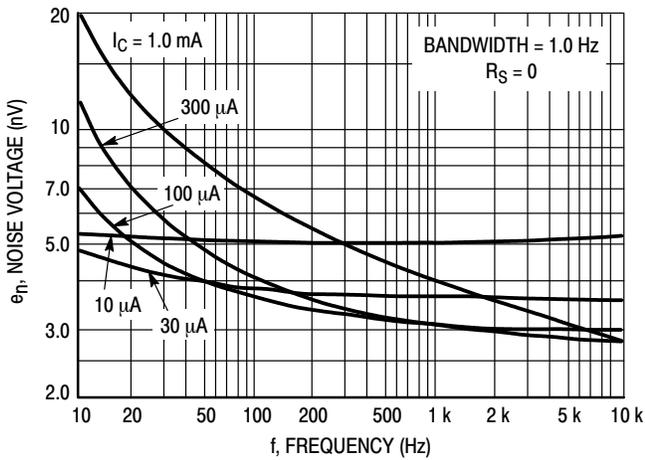


Figure 4. Noise Voltage

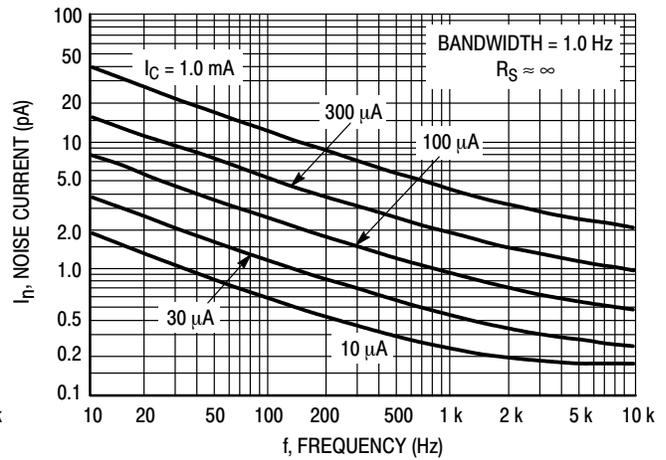


Figure 5. Noise Current

NOISE FIGURE CONTOURS

($V_{CE} = 5.0 \text{ Vdc}$, $T_A = 25^\circ\text{C}$)

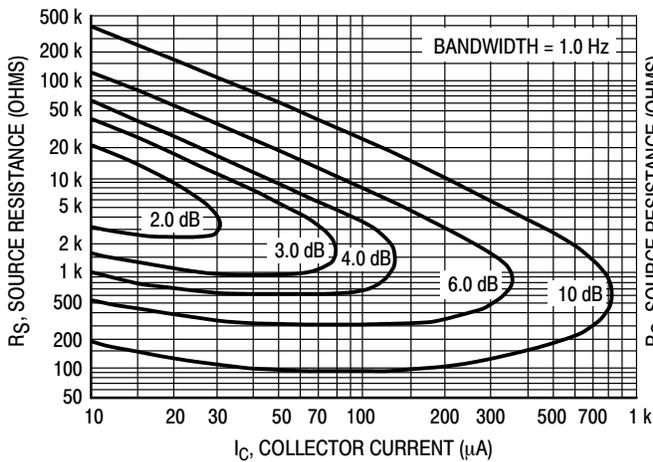


Figure 6. Narrow Band, 100 Hz

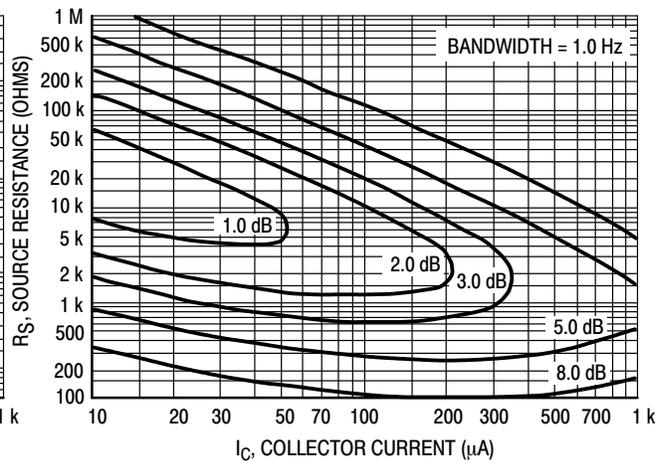


Figure 7. Narrow Band, 1.0 kHz

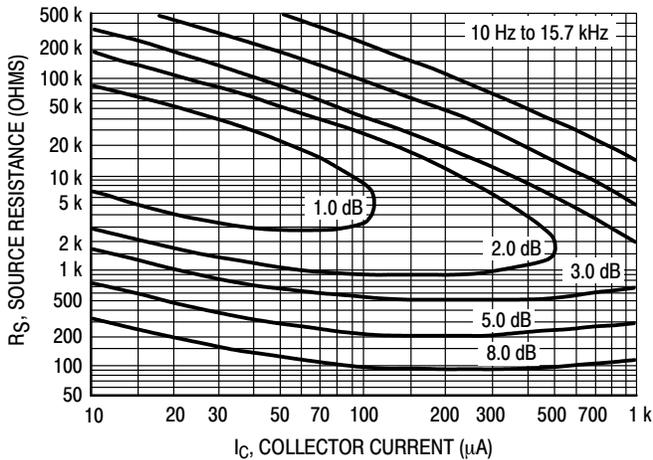


Figure 8. Wideband

Noise Figure is defined as:

$$NF = 20 \log_{10} \left(\frac{e_n^2 + 4KTR_S + I_n^2 R_S^2}{4KTR_S} \right)^{1/2}$$

e_n = Noise Voltage of the Transistor referred to the input. (Figure 3)

I_n = Noise Current of the Transistor referred to the input. (Figure 4)

K = Boltzman's Constant ($1.38 \times 10^{-23} \text{ J}^\circ\text{K}$)

T = Temperature of the Source Resistance ($^\circ\text{K}$)

R_S = Source Resistance (Ohms)

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TYPICAL STATIC CHARACTERISTICS

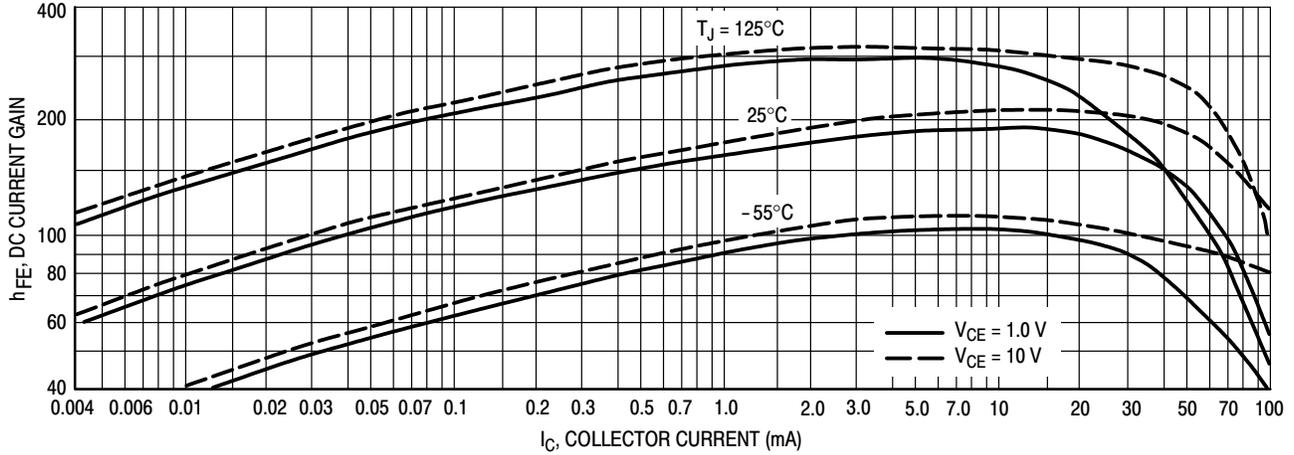


Figure 9. DC Current Gain

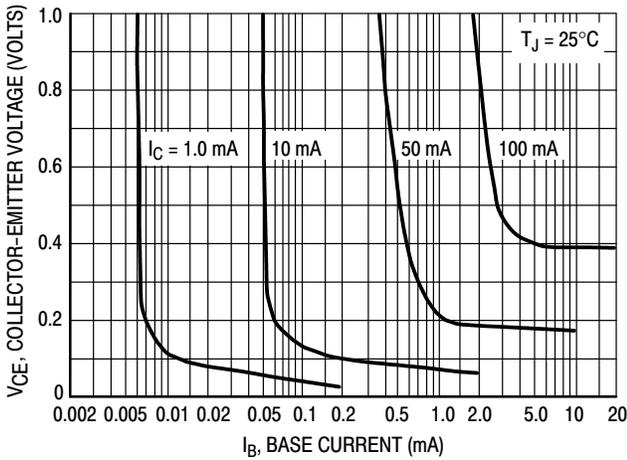


Figure 10. Collector Saturation Region

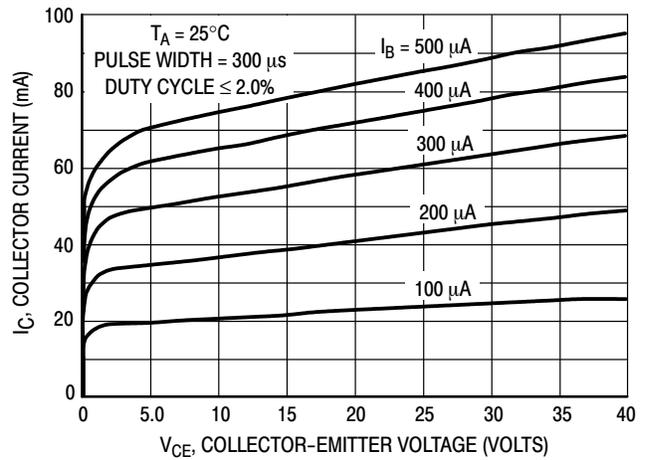


Figure 11. Collector Characteristics

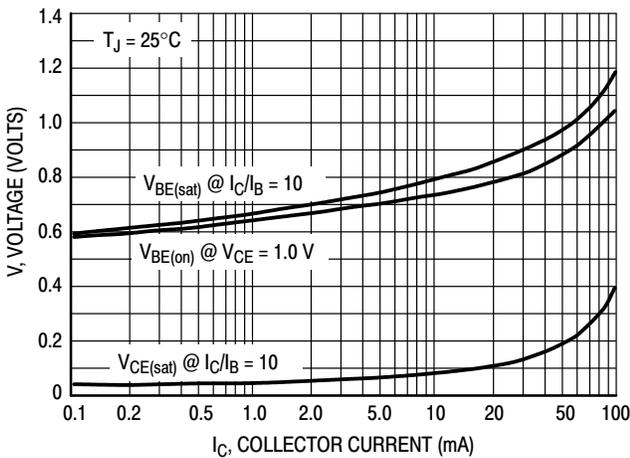


Figure 12. "On" Voltages

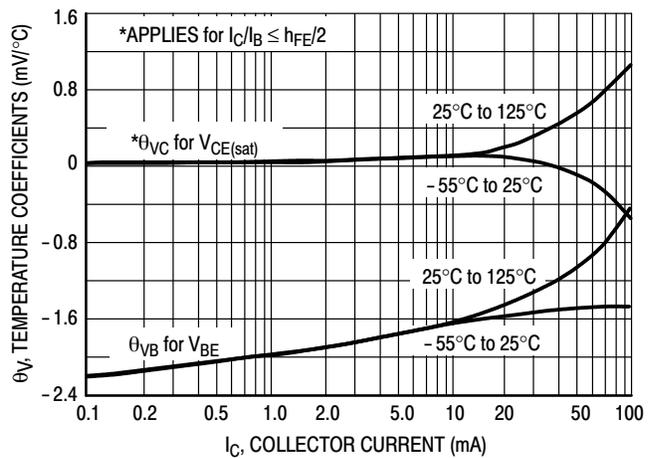


Figure 13. Temperature Coefficients

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TYPICAL DYNAMIC CHARACTERISTICS

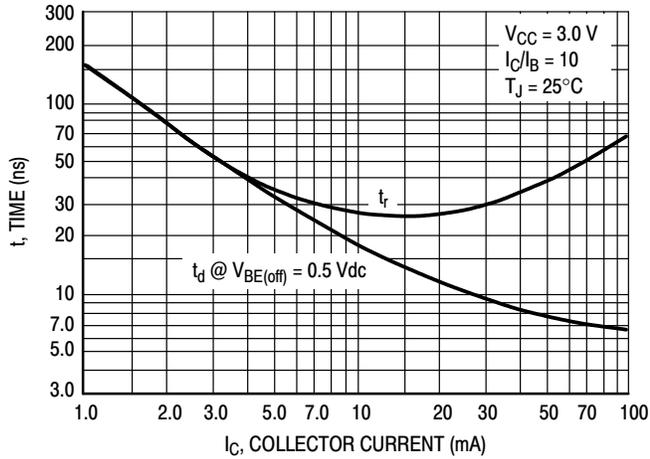


Figure 14. Turn-On Time

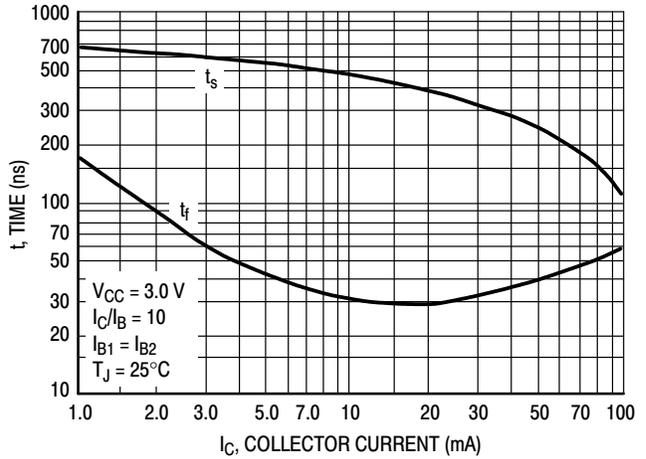


Figure 15. Turn-Off Time

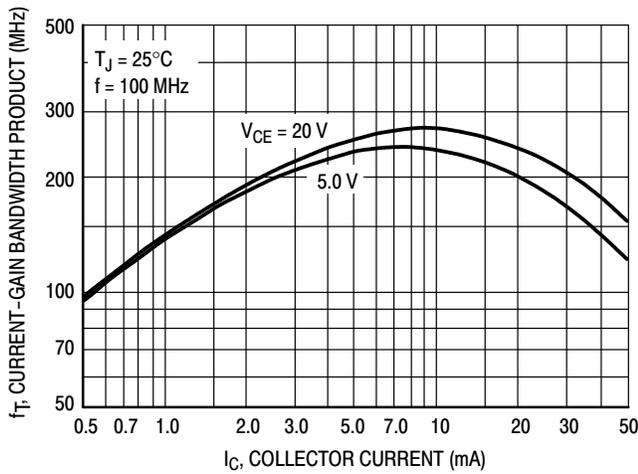


Figure 16. Current-Gain — Bandwidth Product

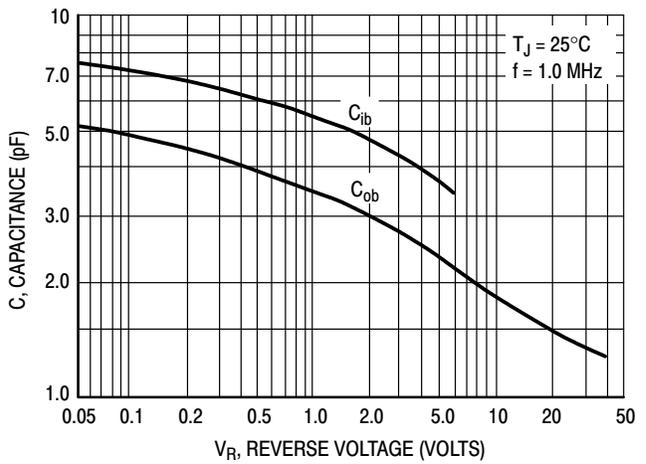


Figure 17. Capacitance

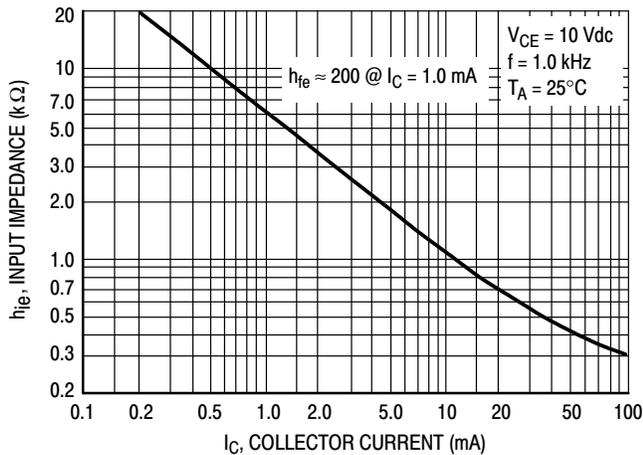


Figure 18. Input Impedance

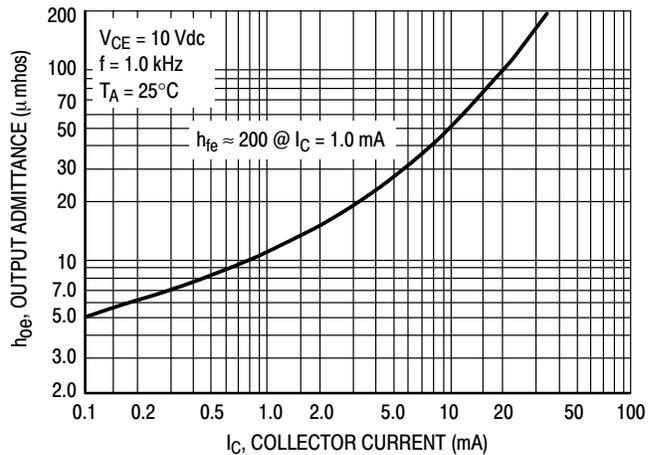


Figure 19. Output Admittance

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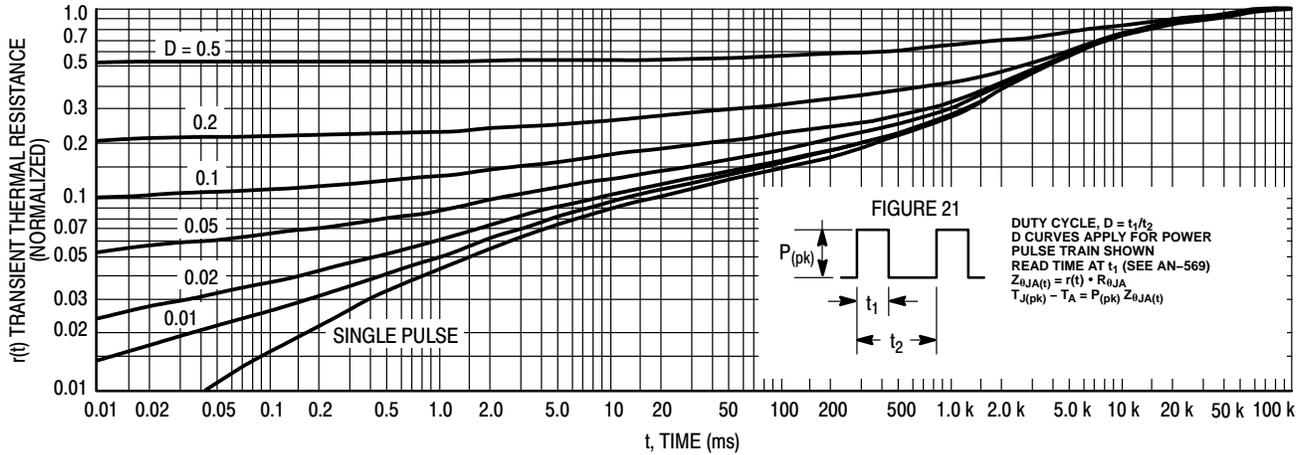


Figure 20. Thermal Response

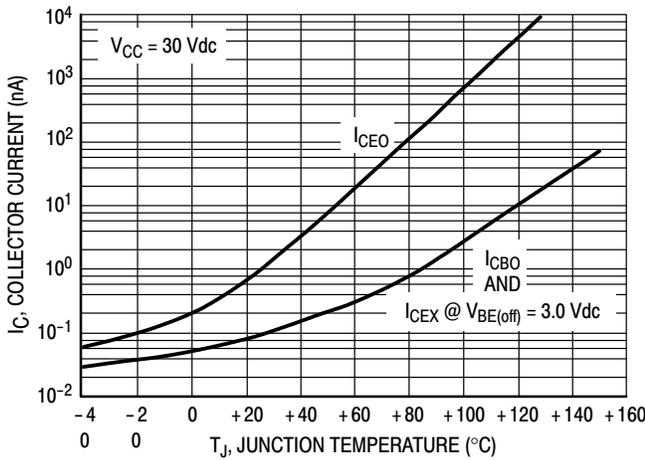


Figure 21.

DESIGN NOTE: USE OF THERMAL RESPONSE DATA

A train of periodical power pulses can be represented by the model as shown in Figure 21. Using the model and the device thermal response the normalized effective transient thermal resistance of Figure 20 was calculated for various duty cycles.

To find $Z_{\theta JA}(t)$, multiply the value obtained from Figure 20 by the steady state value $R_{\theta JA}$.

Example:

The MPS6521 is dissipating 2.0 watts peak under the following conditions:

$t_1 = 1.0$ ms, $t_2 = 5.0$ ms. ($D = 0.2$)

Using Figure 20 at a pulse width of 1.0 ms and $D = 0.2$, the reading of $r(t)$ is 0.22.

The peak rise in junction temperature is therefore

$$\Delta T = r(t) \times P_{(pk)} \times R_{\theta JA} = 0.22 \times 2.0 \times 200 = 88^\circ\text{C}$$

For more information, see ON Semiconductor Application Note AN569/D, available from the Literature Distribution Center or on our website at www.onsemi.com.

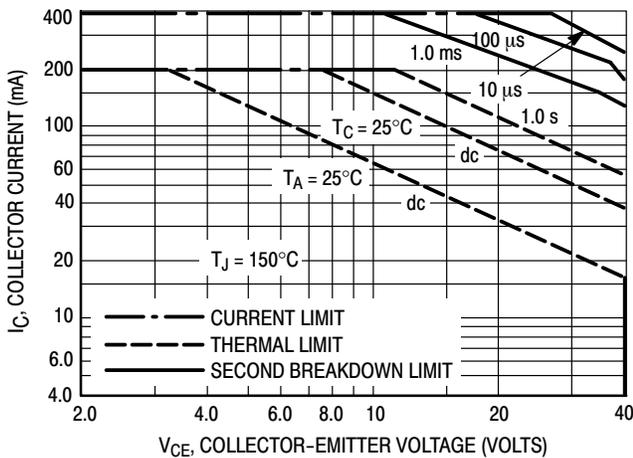


Figure 22.

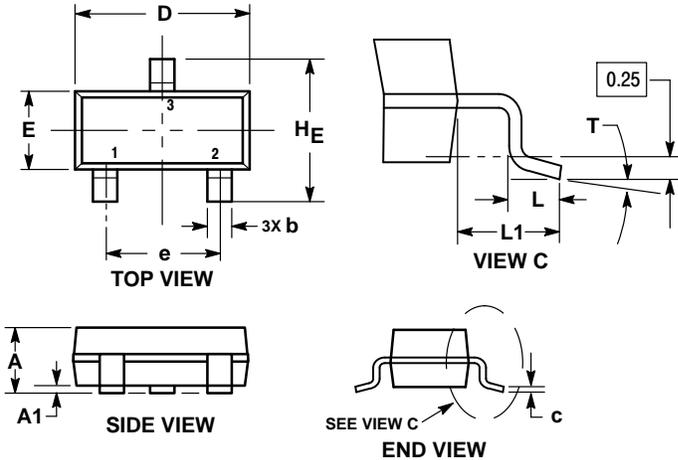
The safe operating area curves indicate I_C - V_{CE} limits of the transistor that must be observed for reliable operation. Collector load lines for specific circuits must fall below the limits indicated by the applicable curve.

The data of Figure 22 is based upon $T_{J(pk)} = 150^\circ\text{C}$; T_C or T_A is variable depending upon conditions. Pulse curves are valid for duty cycles to 10% provided $T_{J(pk)} \leq 150^\circ\text{C}$. $T_{J(pk)}$ may be calculated from the data in Figure 20. At high case or ambient temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

MMBT6521LT1G, SMMBT6521LT1G

PACKAGE DIMENSIONS

SOT-23 (TO-236)
CASE 318-08
ISSUE AR

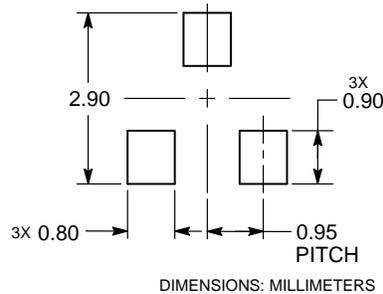


- NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
 2. CONTROLLING DIMENSION: MILLIMETERS.
 3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF THE BASE MATERIAL.
 4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

DIM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.89	1.00	1.11	0.035	0.039	0.044
A1	0.01	0.06	0.10	0.000	0.002	0.004
b	0.37	0.44	0.50	0.015	0.017	0.020
c	0.08	0.14	0.20	0.003	0.006	0.008
D	2.80	2.90	3.04	0.110	0.114	0.120
E	1.20	1.30	1.40	0.047	0.051	0.055
e	1.78	1.90	2.04	0.070	0.075	0.080
L	0.30	0.43	0.55	0.012	0.017	0.022
L1	0.35	0.54	0.69	0.014	0.021	0.027
HE	2.10	2.40	2.64	0.083	0.094	0.104
T	0°	---	10°	0°	---	10°

- STYLE 6:
PIN 1. BASE
2. EMITTER
3. COLLECTOR

RECOMMENDED SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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