# MOSFET - Symmetrical Dual N-Channel 80 V, 18 mΩ, 26 A

# NTTFD018N08LC

# **General Description**

This device includes two specialized N-Channel MOSFETs in a dual package. The switch node has been internally connected to enable easy placement and routing of synchronous buck converters. The control MOSFET (Q2) and synchronous (Q1) have been designed to provide optimal power efficiency.

# **Features**

Q1: N-Channel

- Max  $r_{DS(on)} = 18 \text{ m}\Omega$  at  $V_{GS} = 10 \text{ V}$ ,  $I_D = 7.8 \text{ A}$
- Max  $r_{DS(on)}$  = 29 m $\Omega$  at  $V_{GS}$  = 4.5,  $I_D$  = 6.2 A

Q2: N-Channel

- Max  $r_{DS(on)} = 18 \text{ m}\Omega$  at  $V_{GS} = 10 \text{ V}$ ,  $I_D = 7.8 \text{ A}$
- Max  $r_{DS(on)} = 29 \text{ m}\Omega$  at  $V_{GS} = 4.5$ ,  $I_D = 6.2 \text{ A}$
- Low Inductance Packaging Shortens Rise/Fall Times, Resulting in Lower Switching Losses
- RoHS Compliant

# **Typical Applications**

- 48 V Input Primary Half Bridge
- Communications
- General Purpose Point of Load

# PIN DESCRIPTION

Pin	Name	Description
1, 11, 12	GND (LSS)	Low Side Source
2	LSG	Low Side Gate
3, 4, 5, 6	V + (HSD)	High Side Drain
7	HSG	High Side Gate
8, 9, 10	sw	Switching Node, Low Side Drain

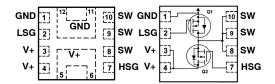


# ON Semiconductor®

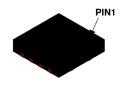
## www.onsemi.com

V <sub>(BR)DSS</sub>	R <sub>DS(ON)</sub> MAX	I <sub>D</sub> MAX
80 V	18 mΩ @ 10 V	26 A
00 V	29 mΩ @ 4.5 V	2014

## **ELECTRICAL CONNECTION**



**Dual N-Channel MOSFET** 





Top

Bottom

Power Clip 33 Symmetric (WQFN12) CASE 510CJ

# **MARKING DIAGRAM**

D018 AYWWZZ

D018 = Specific Device Code
A = Assembly Plant Code
Y = Numeric Year Code
WW = Work Week Code
ZZ = Assembly Lot Code

# **ORDERING INFORMATION**

See detailed ordering and shipping information on page 2 of this data sheet.

# ORDERING INFORMATION AND PACKAGE MARKING

Device	Marking	Package	Shipping <sup>†</sup>
NTTFD018N08LC	D018	WQFN12 (Pb-Free)	3000 Units/ Tape & Reel

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

# MOSFET MAXIMUM RATINGS (T<sub>A</sub> = 25°C, Unless otherwise specified)

Symbol		Paran	neter		Q1	Q2	Units
$V_{DS}$	Drain to Source	Voltage			80	80	V
$V_{GS}$	Gate to Source \	/oltage			±20	±20	V
I <sub>D</sub>	Drain Current	-Continuous	T <sub>C</sub> = 25°C	(Note 4)	26	26	Α
		-Continuous	T <sub>C</sub> = 100°C	(Note 4)	16	16	
		-Continuous	T <sub>A</sub> = 25°C		6 (Note 1a)	6 (Note 1b)	
		-Pulsed	T <sub>A</sub> = 25°C		349	349	
E <sub>AS</sub>	Single Pulse Ava	alanche Energy (L = 1 m	H, I <sub>L(pk)</sub> = 8 A)	(Note 3)	32	32	mJ
$P_{D}$	Power Dissipation	n for Single Operation	T <sub>C</sub> = 25°C		26	26	W
	Power Dissipation	n for Single Operation	T <sub>A</sub> = 25°C		1.7 (Note 1a)	1.7 (Note 1b)	
I <sub>S</sub>	Source Current (	Body Diode)			21	21	Α
T <sub>J</sub> , T <sub>STG</sub>	Operating and Storage Junction Temperature Range		–55 to	+150	°C		
TL	Lead Temperatu	re for Soldering Purpose	es (1/8" from case for 10 s)		260	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

# THERMAL CHARACTERISTICS

Symbol	Parameter	Q1	Q2	Units
$R_{\theta JC}$	Thermal Resistance, Junction to Case	4.8	4.8	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	70 (Note 1a)	70 (Note 1b)	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	135 (Note 1c)	135 (Note 1c)	

# **ELECTRICAL CHARACTERISTICS** (T<sub>J</sub> = 25°C unless otherwise noted)

Symbol	Parameter	Test Conditions	Туре	Min.	Тур.	Max.	Units	
OFF CHAR	OFF CHARACTERISTICS							
BV <sub>DSS</sub>	Drain to Source Breakdown Voltage	$I_D = 250 \mu A, V_{GS} = 0 V$	Q1	80			V	
		$I_D = 250 \mu\text{A},  V_{GS} = 0 \text{V}$	Q2	80				
$\Delta BV_{DSS}$	Breakdown Voltage Temperature	I <sub>D</sub> = 250 μA, referenced to 25°C	Q1		76.81		mV/°C	
$\DeltaT_J$	Coefficient	I <sub>D</sub> = 250 μA, referenced to 25°C	Q2		76.81			
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> = 64 V, V <sub>GS</sub> = 0 V	Q1			1	μΑ	
		V <sub>DS</sub> = 64 V, V <sub>GS</sub> = 0 V	Q2			1		
I <sub>GSS</sub>	Gate to Source Leakage Current, Forward	$V_{GS} = \pm 20 \text{ V}, V_{DS} = 0 \text{ V}$	Q1			±100	μΑ	
		$V_{GS} = \pm 20 \text{ V}, V_{DS} = 0 \text{ V}$	Q2			±100		

# **ELECTRICAL CHARACTERISTICS** ( $T_J = 25^{\circ}C$ unless otherwise noted)

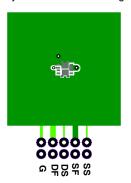
Symbol	Parameter	Test Conditions	Type	Min.	Тур.	Max.	Units
ON CHAR	ACTERISTICS						
V <sub>GS(th)</sub>	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}$ , $I_D = 44 \mu A$	Q1	1.0	1.5	2.5	٧
		$V_{GS} = V_{DS}$ , $I_D = 44 \mu A$	Q2	1.0	1.5	2.5	1
$\Delta V_{GS(th)}$	Gate to Source Threshold Voltage	I <sub>D</sub> = 44 μA, referenced to 25°C	Q1		-5.71		mV/°C
$\Delta T_{J}$	Temperature Coefficient	I <sub>D</sub> = 44 μA, referenced to 25°C	Q2		-5.71		1
r <sub>DS(on)</sub>	Drain to Source On Resistance	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 7.8 A	Q1		15	18	mΩ
		V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 6.2 A			22	29	1
		$V_{GS} = 10 \text{ V}, I_D = 7.8 \text{ A},$ $T_J = 125^{\circ}\text{C}$			25		
r <sub>DS(on)</sub>	Drain to Source On Resistance	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 7.8 A	Q2		15	18	mΩ
		V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 6.2 A			22	29	1
		$V_{GS} = 10 \text{ V}, I_D = 7.8 \text{ A},$ $T_J = 125^{\circ}\text{C}$			25		
9FS	Forward Transconductance	V <sub>DS</sub> = 5 V, I <sub>D</sub> = 7.8 A	Q1		23		S
		V <sub>DS</sub> = 5 V, I <sub>D</sub> = 7.8 A	Q2		23		1
DYNAMIC	CHARACTERISTICS						•
C <sub>ISS</sub>	Input Capacitance	Q1:	Q1		856		pF
		$V_{DS} = 40 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ Mhz}$	Q2		856		1
C <sub>OSS</sub>	Output Capacitance	Q2:	Q1		230		pF
		V <sub>DS</sub> = 40 V, V <sub>GS</sub> = 0 V, f = 1 MHz	Q2		230		1
C <sub>RSS</sub>	Reverse Transfer Capacitance		Q1		10		pF
			Q2		10		1
R <sub>G</sub>	Gate Resistance	T <sub>A</sub> = 25°C	Q1		0.5		Ω
			Q2		0.5		1
SWITCHIN	G CHARACTERISTICS						
td <sub>(ON)</sub>	Turn – On Delay Time	Q1:	Q1		9.4		ns
		$V_{DD}$ = 40 V, $V_{GS}$ = 4.5 V, $I_{D}$ = 6.2 A, $R_{GEN}$ = 6 $\Omega$	Q2		9.4		1
t <sub>r</sub>	Rise Time	Q2:	Q1		5.8		ns
		$V_{DD} = 40 \text{ V}, V_{GS} = 4.5 \text{ V},$	Q2		5.8		1
t <sub>D(OFF)</sub>	Turn – Off Delay Time	$I_D$ = 6.2 A, $R_{GEN}$ = 6 Ω	Q1		14.6		ns
			Q2		14.6		1
t <sub>f</sub>	Fall Time		Q1		5.5		ns
			Q2		5.5		1
Qg	Total Gate Charge	V <sub>GS</sub> = 0V to 10 V	Q1		12.4		nC
			Q2		12.4		1
Qg	Total Gate Charge	V <sub>GS</sub> = 0V to 4.5 V	Q1		6.0		nC
		Q1:	Q2		6.0		
Q <sub>gs</sub>	Gate to Source Gate Charge	$V_{DD} = 40 \text{ V},$	Q1		1.94		nC
-		I <sub>D</sub> = 6.2 A Q2:	Q2		1.94		
Q <sub>gd</sub>	Gate to Drain "Miller" Charge	$V_{DD} = 40 \text{ V},$ $I_{D} = 6.2 \text{ A}$	Q1		1.71		nC
	_	ID - 0.2 A	1	I	1	I	1

# ELECTRICAL CHARACTERISTICS (T<sub>J</sub> = 25°C unless otherwise noted)

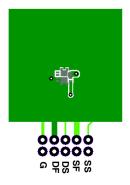
Symbol	Parameter	Test Conditions	Туре	Min.	Тур.	Max.	Units			
DRAIN-SC	DRAIN-SOURCE DIODE CHARACTERISTICS									
V <sub>SD</sub>	Source to Drain Diode Forward Voltage	V <sub>GS</sub> = 0 V, I <sub>S</sub> = 7.8 A (Note 2)	Q1		0.82	1.5	V			
		V <sub>GS</sub> = 0 V, I <sub>S</sub> = 7.8 A (Note 2)	Q2		0.82	1.5				
t <sub>rr</sub>	Reverse Recovery Time	Q1:	Q1		13.3		ns			
		I <sub>F</sub> = 7.8 A, di/dt = 300 A/μs	Q2		13.3					
Q <sub>rr</sub>	Reverse Recovery Charge	Q2: I <sub>F</sub> = 7.8 A, di/dt = 300 A/μs	Q1		18.1		nC			
			Q2		18.1					
t <sub>rr</sub>	Reverse Recovery Time	Q1:	Q1		10.3		ns			
		I <sub>F</sub> = 7.8 A, di/dt = 1000 A/μs	Q2		10.3					
Q <sub>rr</sub>	Reverse Recovery Charge	-Q2: I <sub>F</sub> = 7.8 A, di/dt = 1000 A/μs	Q1		51		nC			
			Q2		51					

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

1.  $R_{\theta JA}$  is determined with the device mounted on a 1 in<sup>2</sup> pad 2 oz copper pad on a 1.5  $\times$  1.5 in. board of FR-4 material.  $R_{\theta CA}$  is determined by the user's board design.



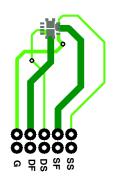
a) 70°C/W when mounted on a 1 in<sup>2</sup> pad of 2 oz copper.



b) 70°C/W when mounted on a 1 in<sup>2</sup> pad of 2 oz copper.



c) 135°C/W when mounted on a minimum pad of 2 oz copper.



d) 135°C/W when mounted on a minimum pad of 2 oz copper.

- Pulse Test: Pulse Width < 300 μs, Duty cycle < 2.0%.</li>
   Q1: E<sub>AS</sub> of 32 mJ is based on starting T<sub>J</sub> = 25°C; N-ch: L = 1 mH, I<sub>AS</sub> = 8 A, V<sub>DD</sub> = 80 V, V<sub>GS</sub> = 10 V. 100% test at L = 1 mH, I<sub>AS</sub> = 8.2 A. Q2: E<sub>AS</sub> of 32 mJ is based on starting T<sub>J</sub> = 25°C; N-ch: L = 1 mH, I<sub>AS</sub> = 8 A, V<sub>DD</sub> = 80 V, V<sub>GS</sub> = 10 V. 100% test at L = 1 mH, I<sub>AS</sub> = 8.2 A.
   Computed continuous current limited to Max Junction Temperature only, actual continuous current will be limited by thermal
- & electro-mechanical application board design.

# **TYPICAL CHARACTERISTICS**

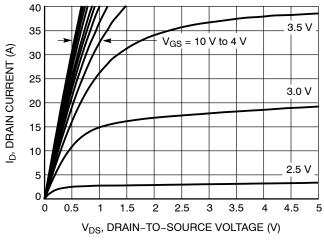


Figure 1. On-Region Characteristics

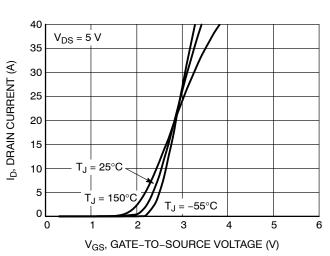


Figure 2. Transfer Characteristics

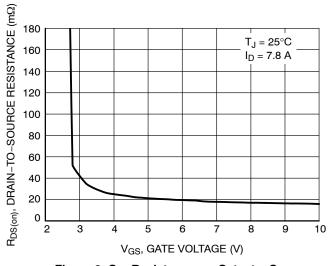


Figure 3. On-Resistance vs. Gate-to-Source Voltage

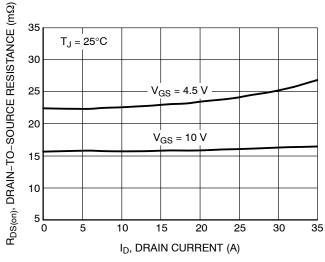


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

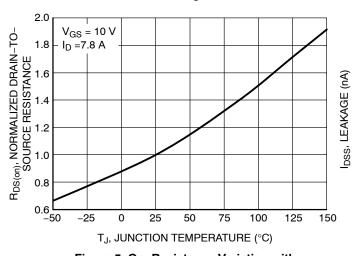


Figure 5. On–Resistance Variation with Temperature

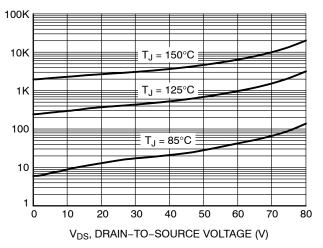


Figure 6. Drain-to-Source Leakage Current vs. Voltage

# **TYPICAL CHARACTERISTICS**

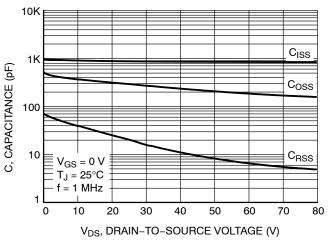


Figure 7. Capacitance Variation

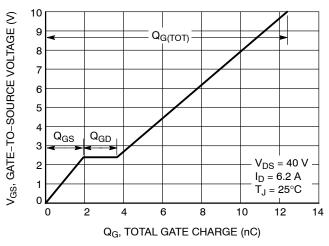


Figure 8. Gate-to-Source and Drain-to-Source Voltage vs. Total Charge

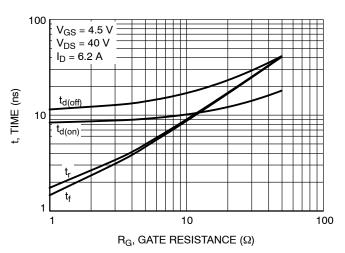


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

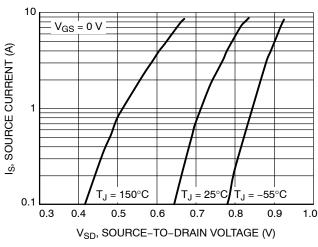


Figure 10. Diode Forward Voltage vs. Current

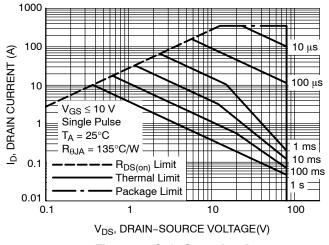


Figure 11. Safe Operating Area

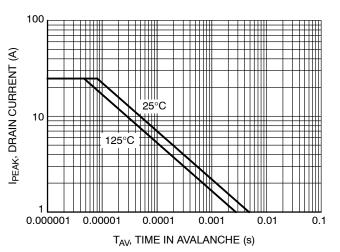


Figure 12. I<sub>PEAK</sub> vs. Time in Avalanche

# **TYPICAL CHARACTERISTICS**

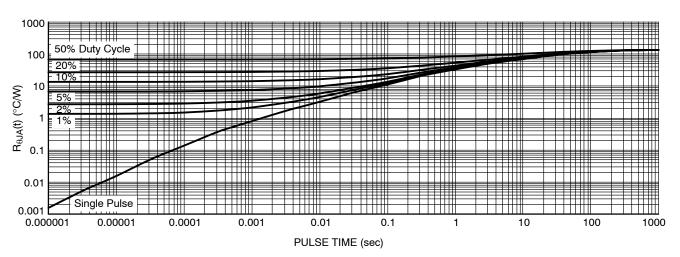


Figure 13. Thermal Characteristics

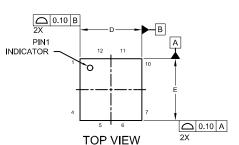




# WQFN12 3.3X3.3, 0.65P CASE 510CJ **ISSUE A**

**DATE 08 AUG 2022** 

MILLIMETERS



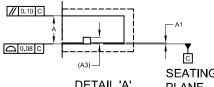
FRONT VIEW

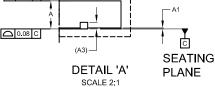
D2 (2x)

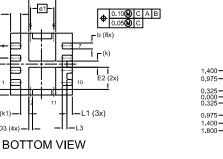
E3 (4x)

#### NOTES:

- 1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
- CONTROLLING DIMENSION: MILLIMETERS
- COPLANARITY APPLIES TO THE EXPOSED
- 4. SEATING PLANE IS DEFINED BY THE TERMINALS. "A1" IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.
- 5. IT IS RECOMMENDED TO HAVE NO TRACES OR VIAS WITHIN THE KEEP OUT AREA.

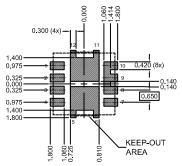






SEE

**DETAIL A** 



DIM MIN NOM MAX 0.70 0.75 0.80 Α 0.00 A1 0.05 АЗ 0.20 REF 0.27 0.32 0.37 b D 3.30 3.40 3.20 D2 1.34 1.44 1.54 D3 0.10 0.20 0.30 Ε 3.20 3.30 3.40 1.09 1.29 F2 1.19 E3 0.20 0.30 0.40 е 0.65 BSC 0.325 BSC e/2 1.24 BSC е1 k 0.33 REF k1 0.43 REF 0.44 0.54 L 0.64 L1 0.19 0.29 0.39 L3 0.15 0.25 0.35

# **GENERIC MARKING DIAGRAM\***



XXXX = Specific Device Code = Assembly Location = Year

WW = Work Week

= Pb-Free Package

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "", may or may not be present. Some products may not follow the Generic Marking.

LAND PATTERN
RECOMMENDATION
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PB-FREE STRATEGY AND SOLDERING
DETAILS, PLEASE DOWNLOAD THE ON
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MOUNTING TECHNIQUES REFERENCE
MANUAL, SOLDERRM/D.

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DESCRIPTION:	WQFN12 3.3X3.3, 0.65P		PAGE 1 OF 1	

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