NSP8814, NSP8818

ESD and Surge Protection Device

Low Capacitance Surge Protection for High Speed Data

The NSP8814 and NSP8818 surge protectors are designed specifically to protect 10/100 and GbE Ethernet signals from high levels of surge current. Low clamping voltage under high surge conditions make this device an ideal solution for protecting voltage sensitive lines leading to Ethernet transceiver chips. Low capacitance combined with flow-through style packaging allows for easy PCB layout and matched trace lengths necessary to maintain consistent impedance between high-speed differential lines.

Features

- Protection for the Following IEC Standards:
  IEC 61000−4−2 (ESD) ±30 kV (Contact)
  IEC 61000−4−5 (Lightning) 35 A (8/20 μs)
- Flow−Thru Routing Scheme
- Low Capacitance: 2 pF Max (I/O to I/O)
- UL Flammability Rating of 94 V−0
- SZ Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q101 Qualified and PPAP Capable*
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

Typical Applications

- 10/100 and GbE Ethernet
- MagJacks® / Integrated Magnetics
- Notebooks/Desktops/Servers

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Operating Junction Temperature Range	T_J	−55 to +125	°C
Storage Temperature Range	T_{stg}	−55 to +150	°C
Lead Solder Temperature − Maximum (10 Seconds)	T_L	260	°C
IEC 61000−4−2 Contact (ESD) IEC 61000−4−2 Air (ESD) ISO 10605 330 pF / 330 Ω Contact ISO 10605 330 pF / 2 kΩ Contact ISO 10605 150 pF / 2 kΩ Contact	ESD	±30 ±30 ±30 ±30 ±30	kV
Maximum Peak Pulse Current 8/20 μs @ T_A = 25°C 10/700 μs @ T_A = 25°C	I_{PP}	 35 20	A

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

See Application Note AND8308/D for further description of survivability specs.

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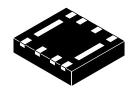
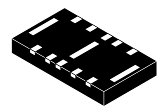
MARKING DIAGRAMS



UDFN8
CASE 506CV

4C M
▪



UDFN10
CASE 506CU

4D M
▪

XX = Specific Device Code
M = Date Code
▪ = Pb−Free Package

ORDERING INFORMATION

Device	Package	Shipping
NSP8814MUTAG	UDFN8 (Pb−Free)	3000 / Tape & Reel
SZNSP8814MUTAG	UDFN8 (Pb−Free)	3000 / Tape & Reel
NSP8818MUTAG	UDFN10 (Pb−Free)	3000 / Tape & Reel
SZNSP8818MUTAG	UDFN10 (Pb−Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

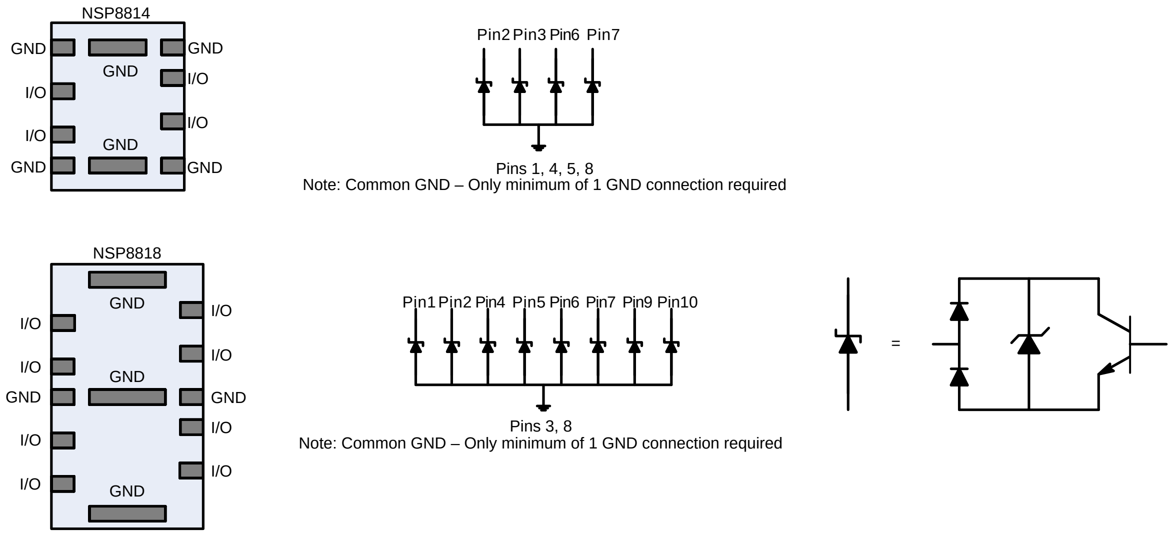
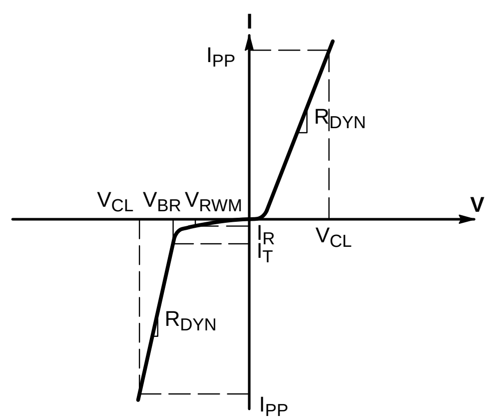


Figure 1. Pin Schematic

ELECTRICAL CHARACTERISTICS

(T_A = 25°C unless otherwise noted)

Symbol	Parameter
V_{RWM}	Working Peak Voltage
I_R	Maximum Reverse Leakage Current @ V_{RWM}
V_{BR}	Breakdown Voltage @ I_T
I_T	Test Current
V_{HOLD}	Holding Reverse Voltage
I_{HOLD}	Holding Reverse Current
R_{DYN}	Dynamic Resistance
I_{PP}	Maximum Peak Pulse Current
V_C	Clamping Voltage @ I_{PP} $V_C = V_{HOLD} + (I_{PP} * R_{DYN})$



Uni−Directional Surge Protection

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise specified)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Reverse Working Voltage	V_{RWM}	Any I/O to GND (Note 1)			3.0	V
Forward Voltage	V_F	I_F = 10 mA, GND to All IO Pins	0.5	0.85	1.1	V
Breakdown Voltage	V_{BR}	I_T = 1 mA, I/O to GND	3.2	3.5	5.0	V
Reverse Leakage Current	I_R	V_{RWM} = 3.0 V, I/O to GND			0.5	μA
Clamping Voltage (Note 2)	V_C	I_{PP} = 1 A			5.0	V
		I_{PP} = 10 A			6.0	
		I_{PP} = 25 A			10	
		I_{PP} = 35 A			15	
Clamping Voltage	V_C	IEC61000−4−2, ±8 kV Contact		See Figures 7 and 14		
Junction Capacitance	C_J	V_R = 0 V, f = 1 MHz between I/O Pins		1.5	2.0	pF
		V_R = 0 V, f = 1 MHz between I/O Pins and GND			5.0	

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

1. Surge protection devices are normally selected according to the working peak reverse voltage (V_{RWM}), which should be equal or greater than the DC or continuous peak operating voltage level.
2. Any I/O to GND (8/20 μs pulse).

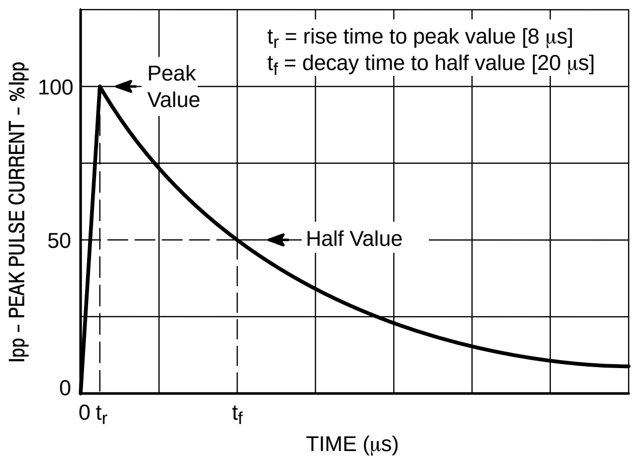


Figure 2. IEC61000−4−5 8/20 μs Pulse Waveform

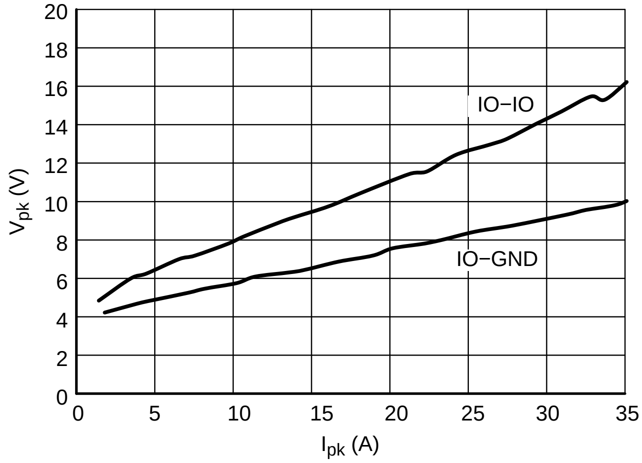


Figure 3. Clamping Voltage vs. Peak Pulse Current (t_p = 8/20 μs per Figure 2)

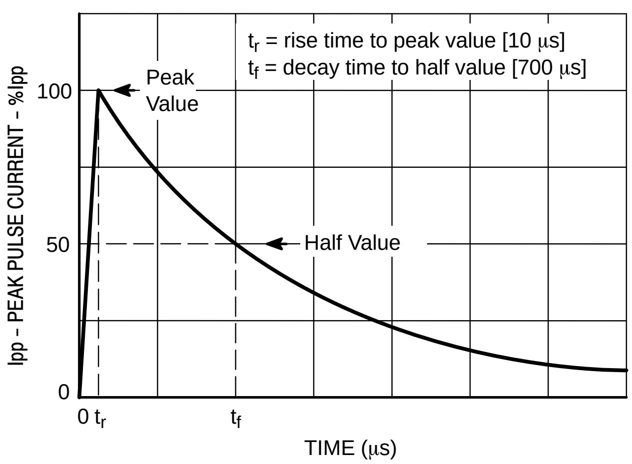


Figure 4. IEC61000−4−5 10/700 μs Pulse Waveform

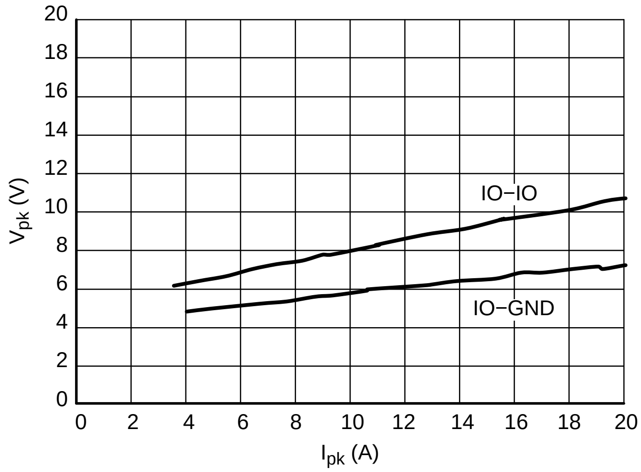


Figure 5. Clamping Voltage vs. Peak Pulse Current (t_p = 10/700 μs per Figure 4)

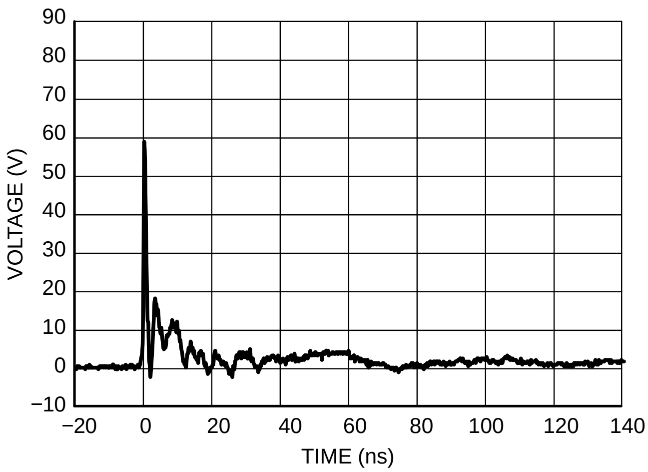


Figure 6. IEC61000−2−4 +8 kV Contact Clamping Voltage

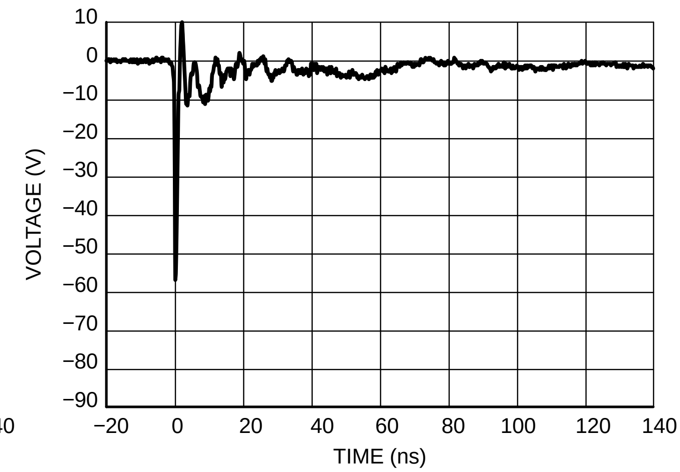


Figure 7. IEC61000−2−4 −8 kV Contact Clamping Voltage

IEC 61000−4−2 Spec.

Level	Test Voltage (kV)	First Peak Current (A)	Current at 30 ns (A)	Current at 60 ns (A)
1	2	7.5	4	2
2	4	15	8	4
3	6	22.5	12	6
4	8	30	16	8

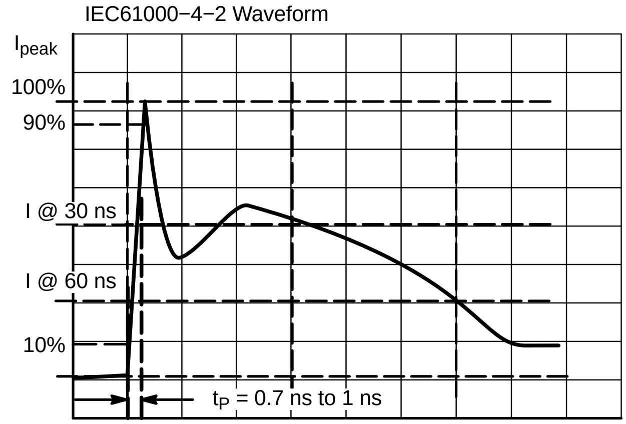


Figure 8. IEC61000−4−2 Spec

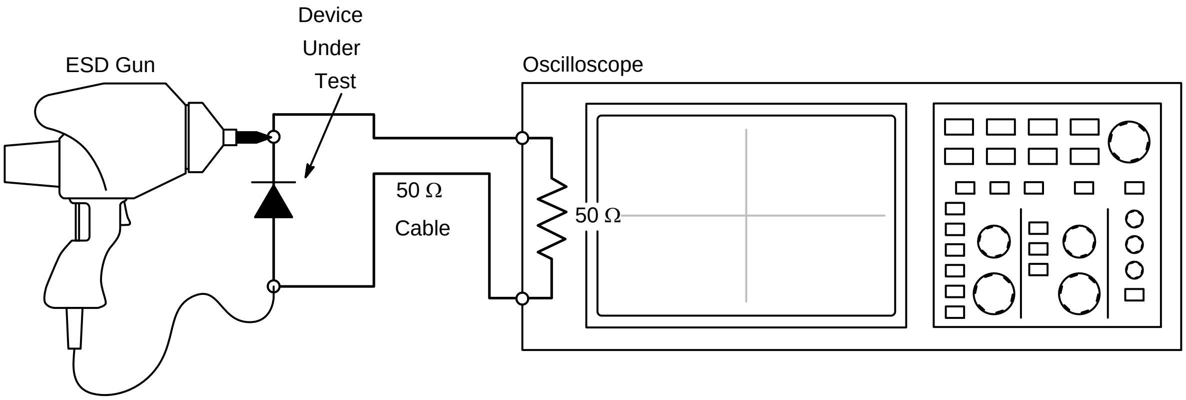


Figure 9. Diagram of ESD Clamping Voltage Test Setup

The following is taken from Application Note AND8308/D − Interpretation of Datasheet Parameters for ESD Devices.

ESD Voltage Clamping

For sensitive circuit elements it is important to limit the voltage that an IC will be exposed to during an ESD event to as low a voltage as possible. The ESD clamping voltage is the voltage drop across the ESD protection diode during an ESD event per the IEC61000−4−2 waveform. Since the IEC61000−4−2 was written as a pass/fail spec for larger systems such as cell phones or laptop computers it is not clearly defined in the spec how to specify a clamping voltage at the device level. ON Semiconductor has developed a way to examine the entire voltage waveform across the ESD protection diode over the time domain of an ESD pulse in the form of an oscilloscope screenshot, which can be found on the datasheets for all ESD protection diodes. For more information on how ON Semiconductor creates these screenshots and how to interpret them please refer to AND8307/D.

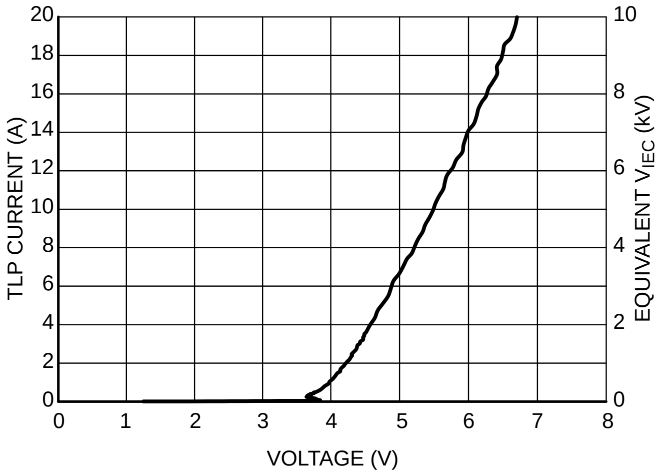


Figure 10. Positive TLP IV Curve

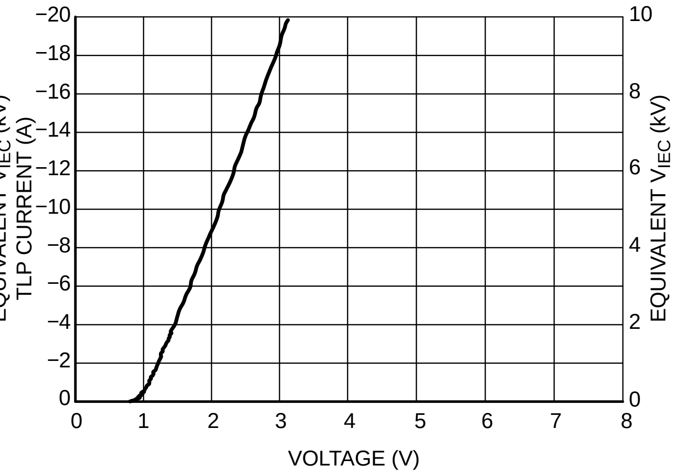


Figure 11. Negative TLP IV Curve

NOTE: TLP parameter: Z_0 = 50 Ω, t_p = 100 ns, t_r = 300 ps, averaging window: t_1 = 30 ns to t_2 = 60 ns.

Transmission Line Pulse (TLP) Measurement

Transmission Line Pulse (TLP) provides current versus voltage (I−V) curves in which each data point is obtained from a 100 ns long rectangular pulse from a charged transmission line. A simplified schematic of a typical TLP system is shown in Figure 12. TLP I−V curves of ESD protection devices accurately demonstrate the product's ESD capability because the 10s of amps current levels and under 100 ns time scale match those of an ESD event. This is illustrated in Figure 13 where an 8 kV IEC 61000−4−2 current waveform is compared with TLP current pulses at 8 A and 16 A. A TLP I−V curve shows the voltage at which the device turns on as well as how well the device clamps voltage over a range of current levels.

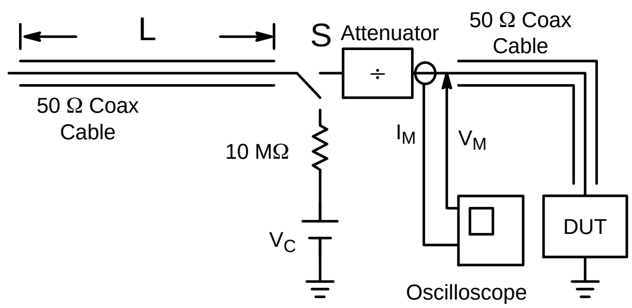


Figure 12. Simplified Schematic of a Typical TLP System

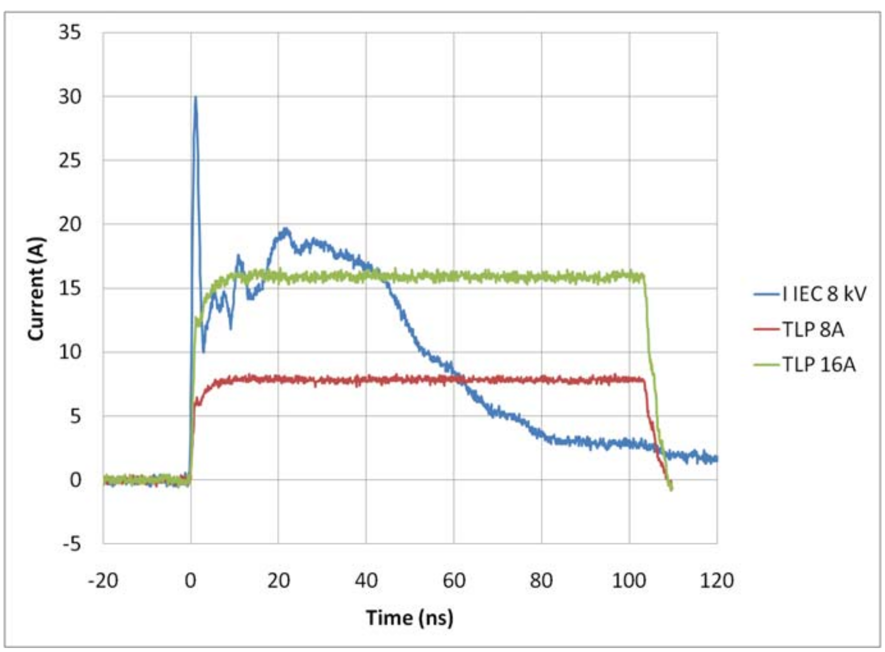


Figure 13. Comparison Between 8 kV IEC 61000−4−2 and 8 A and 16 A TLP Waveforms

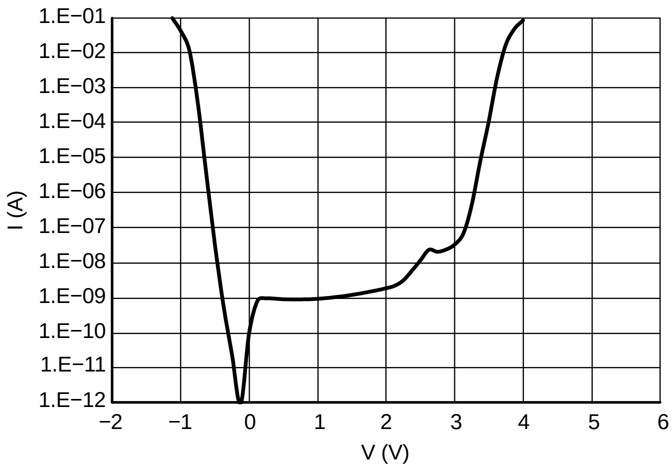


Figure 14. IV Characteristics

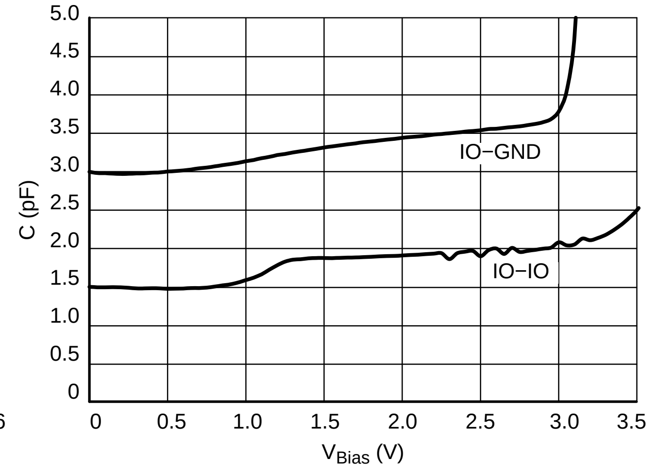


Figure 15. CV Characteristics

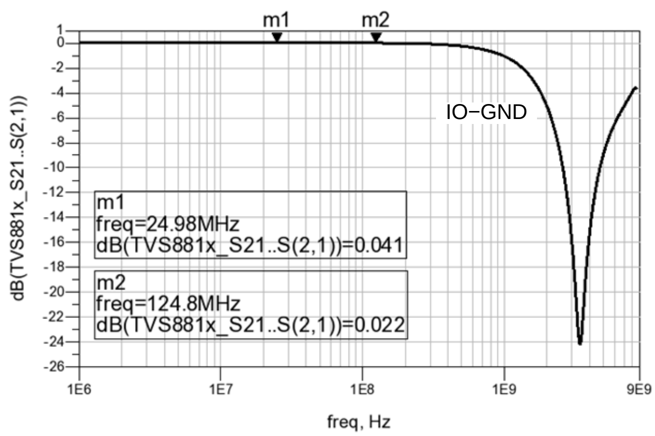


Figure 16. RF Insertion Loss

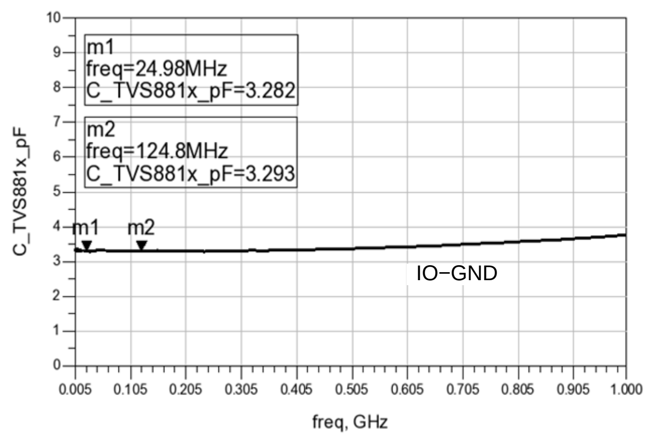


Figure 17. Capacitance Over Frequency

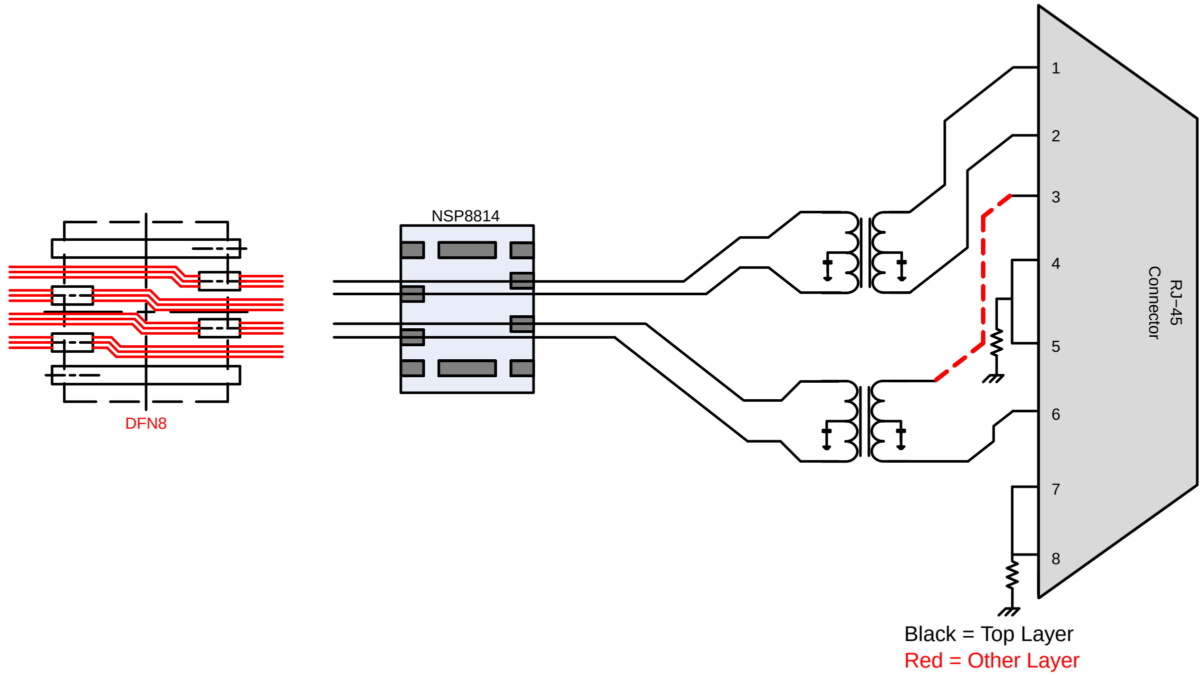


Figure 18. 10/100 Ethernet Layout Diagram and Flow−thru Routing Scheme

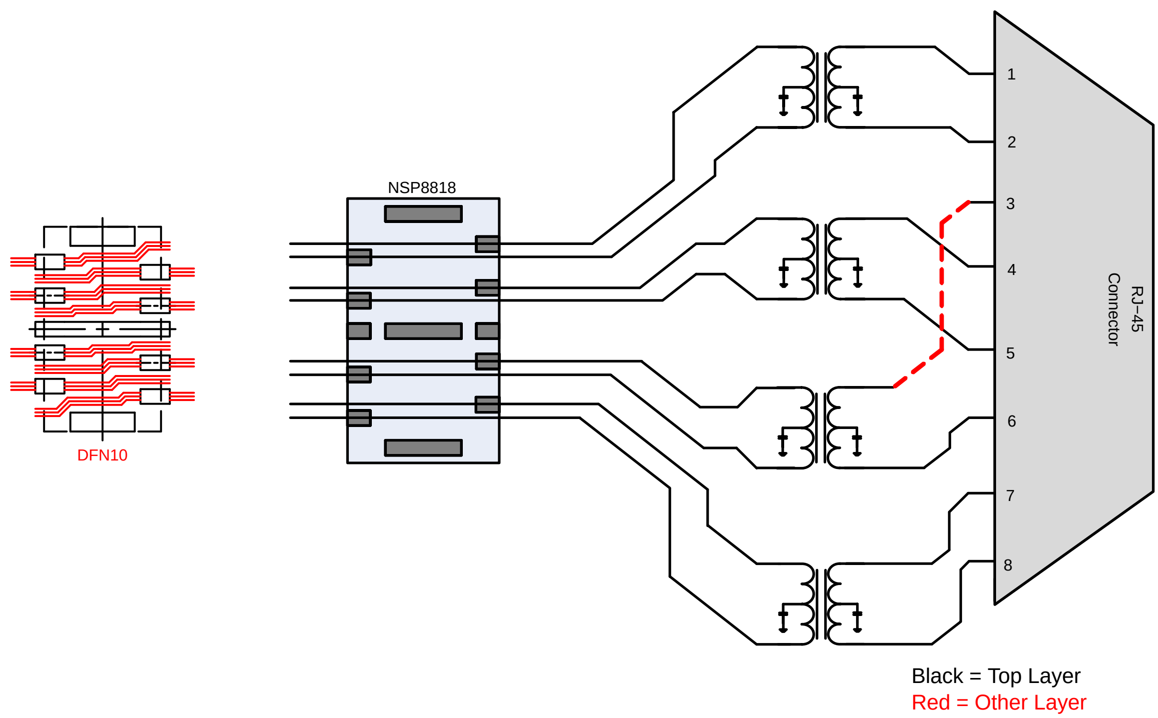
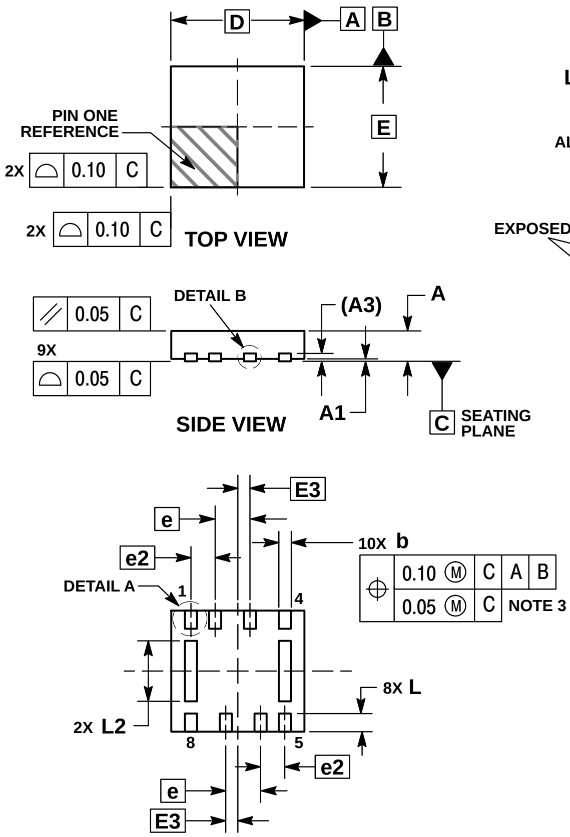


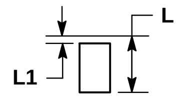
Figure 19. GbE Ethernet Layout Diagram and Flow−thru Routing Scheme

PACKAGE DIMENSIONS

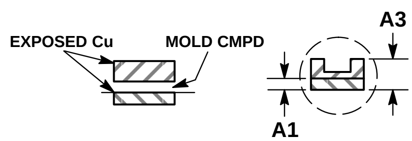
UDFN8 2.2x2, 0.575P
CASE 506CV
ISSUE A



BOTTOM VIEW



DETAIL A
ALTERNATE TERMINAL CONSTRUCTION

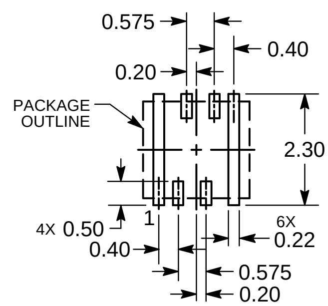


DETAIL B
ALTERNATE CONSTRUCTIONS

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSIONS b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.25 MM FROM TERMINAL TIP.

DIM	MILLIMETERS MIN	MILLIMETERS MAX
A	0.45	0.55
A1	0.00	0.05
A3	0.127 REF	
b	0.15	0.25
D	2.20 BSC	
E	2.00 BSC	
E3	0.20 BSC	
e	0.575 BSC	
e2	0.40 BSC	
L	0.25	0.35
L1	0.05	0.15
L2	0.95	1.05

RECOMMENDED MOUNTING FOOTPRINT

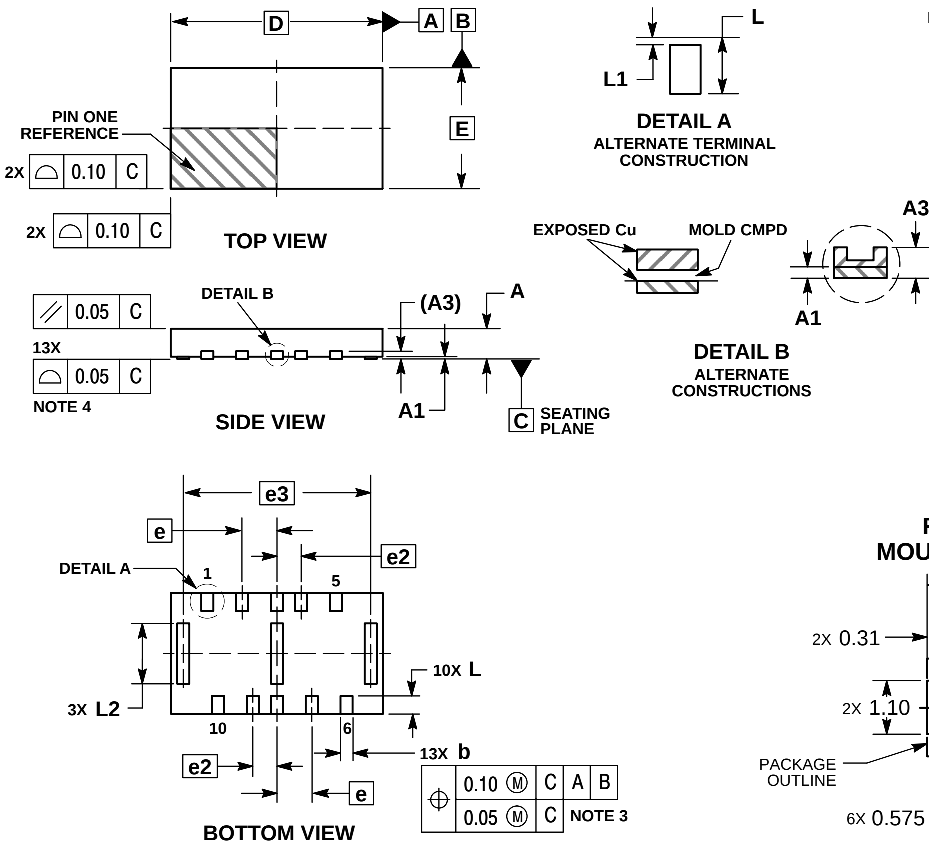


DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PACKAGE DIMENSIONS

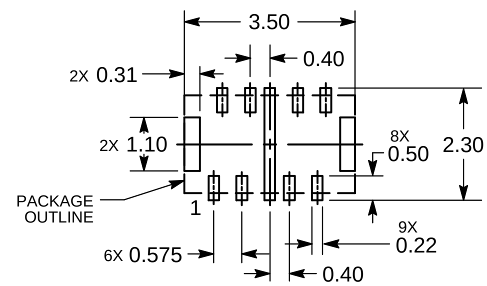
UDFN10 3.5x2, 0.575P
CASE 506CU
ISSUE O



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSIONS b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.25 MM FROM TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.45	0.55
A1	0.00	0.05
A3	0.127 REF	
b	0.15	0.25
D	3.50 BSC	
E	2.00 BSC	
e	0.575 BSC	
e2	0.40 BSC	
e3	3.10 BSC	
L	0.25	0.35
L1	0.05	0.15
L2	0.95	1.05

RECOMMENDED MOUNTING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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