Features

- ESD protection for two lines with bi-directional
- Provide transient protection for each line to
  IEC 61000-4-2 (ESD) ±30kV (air), ±30kV (contact)
  IEC 61000-4-4 (EFT) 80A (5/50ns)
  IEC 61000-4-5 (Lightning) 8A (8/20μs)
  Cable Discharge Event (CDE)
- Ultra-small DFN1006P3X package saves board space
- Protect two I/O lines or two power lines
- Fast turn-on and low clamping voltage
- Low operating voltage: 3.3V maximum
- Solid-state silicon-avalanche and active circuit triggering technology
- ***Green part***

Applications

- Mobile phones
- Hand held portable applications
- Computer interfaces protection
- Microprocessors protection
- Serial and parallel ports protection
- Control signal lines protection
- Power lines on PCB protection
- Latch-up protection

Description

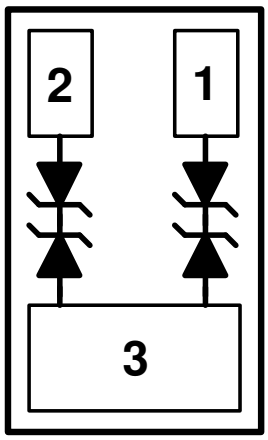
AZ5123-02F is a design which includes two bi-directional ESD rated clamping cells to protect two power lines, or two control lines, or two low-speed data lines in an electronic system. The AZ5123-02F has been specifically designed to protect sensitive components which are connected to power and control lines from over-voltage damage and latch-up caused by Electrostatic Discharging (ESD), Electrical Fast Transients (EFT), and Cable Discharge Event (CDE).

AZ5123-02F is a unique design which includes proprietary clamping cells in a single package. During transient conditions, the proprietary clamping cells prevent over-voltage on the power lines or control/data lines, protecting any downstream components.

AZ5123-02F is bi-directional and may be used on lines where the signal swings above and below ground.

AZ5123-02F may be used to meet the ESD immunity requirements of IEC 61000-4-2, Level 4 (±15kV air, ±8kV contact discharge).

Circuit Diagram / Pin Configuration



DFN1006P3X (Bottom View)

SPECIFICATIONS

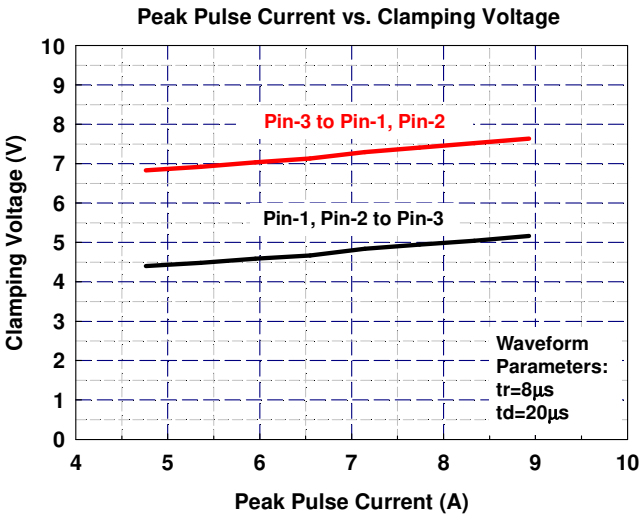
ABSOLUTE MAXIMUM RATINGS (T_A= 25°C, unless otherwise specified)			
PARAMETER	**SYMBOL**	**RATING**	**UNIT**
Peak Pulse Current (tp=8/20μs)	I_{PP}	8	A
Operating Supply Voltage	V_{DC}	±3.6	V
ESD per IEC 61000-4-2 (Air) ESD per IEC 61000-4-2 (Contact)	V_{ESD-1} V_{ESD-2}	±30 ±30	kV
Lead Soldering Temperature	T_{SOL}	260 (10 sec.)	°C
Operating Temperature	T_{OP}	-40 to +85	°C
Storage Temperature	T_{STO}	-55 to +150	°C

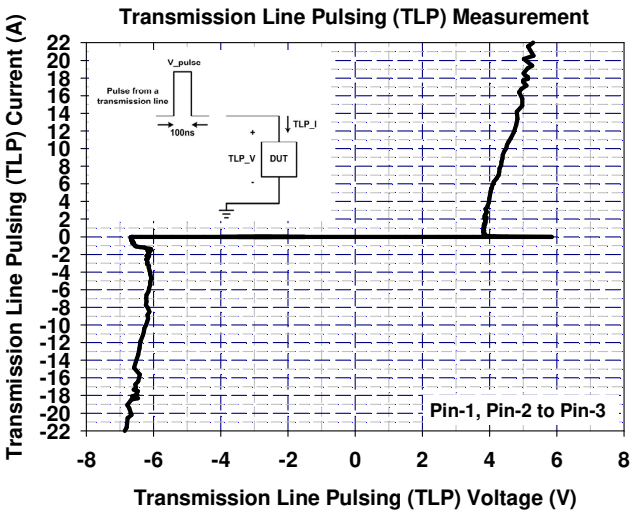
ELECTRICAL CHARACTERISTICS						
PARAMETER	**SYMBOL**	**CONDITION**	**MIN**	**TYP**	**MAX**	**UNIT**
Reverse Stand-Off Voltage	V_{RWM}	T=25 °C	-3.3		3.3	V
Reverse Leakage Current	I_{Leak}	V_{RWM} = ±3.3V, T=25 °C			0.5	μA
Reverse Breakdown Voltage	V_{BV}	I_{BV} = ±1mA, T=25 °C	3.8		6.8	V
Surge Clamping Voltage	$V_{CL-surge}$	I_{PP} = ±5A, tp= 8/20μs, T=25 °C		7		V
ESD Clamping Voltage (Note 1)	V_{CL-ESD}	IEC 61000-4-2 +8kV (I_{TLP}= 16A), Contact mode, T=25 °C		6.5		V
ESD Dynamic Turn-on Resistance	$R_{dynamic}$	IEC 61000-4-2 0~+8kV, Contact mode, T=25 °C		0.07		Ω
Channel Input Capacitance	C_{IN}	V_R = 0V, f = 1MHz, T=25 °C		20	25	pF

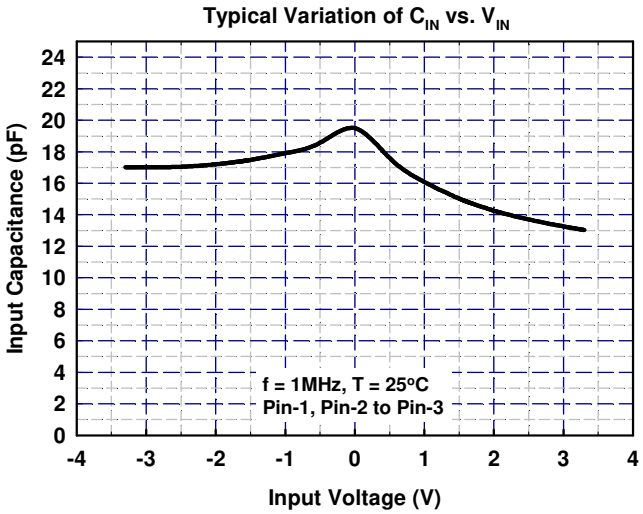
Note 1: ESD Clamping Voltage was measured by Transmission Line Pulsing (TLP) System.

TLP conditions: Z_0= 50Ω, t_p= 100ns, t_r= 1ns.

Typical Characteristics







Application Information

The AZ5123-02F is designed to protect two lines against system ESD/EFT/lightning pulses by clamping it to an acceptable reference. It provides bi-directional protection.

The usage of the AZ5123-02F is shown in Fig. 1. Protected lines, such as data lines, control lines, or power lines, are connected at pin 1 and pin2, respectively. The pin 3 is connected to a ground plane on the board. In order to minimize parasitic inductance in the board traces, all path lengths connected to the pins of AZ5123-02F should be kept as short as possible.

In order to obtain enough suppression of ESD induced transient, a good circuit board is critical. Thus, the following guidelines are recommended:

- Minimize the path length between the protected lines and the AZ5123-02F.
- Place the AZ5123-02F near the input terminals or connectors to restrict transient coupling.
- The ESD current return path to ground should be kept as short as possible.
- Use ground planes whenever possible.
- NEVER route critical signals near board edges and near the lines which the ESD transient easily injects to.

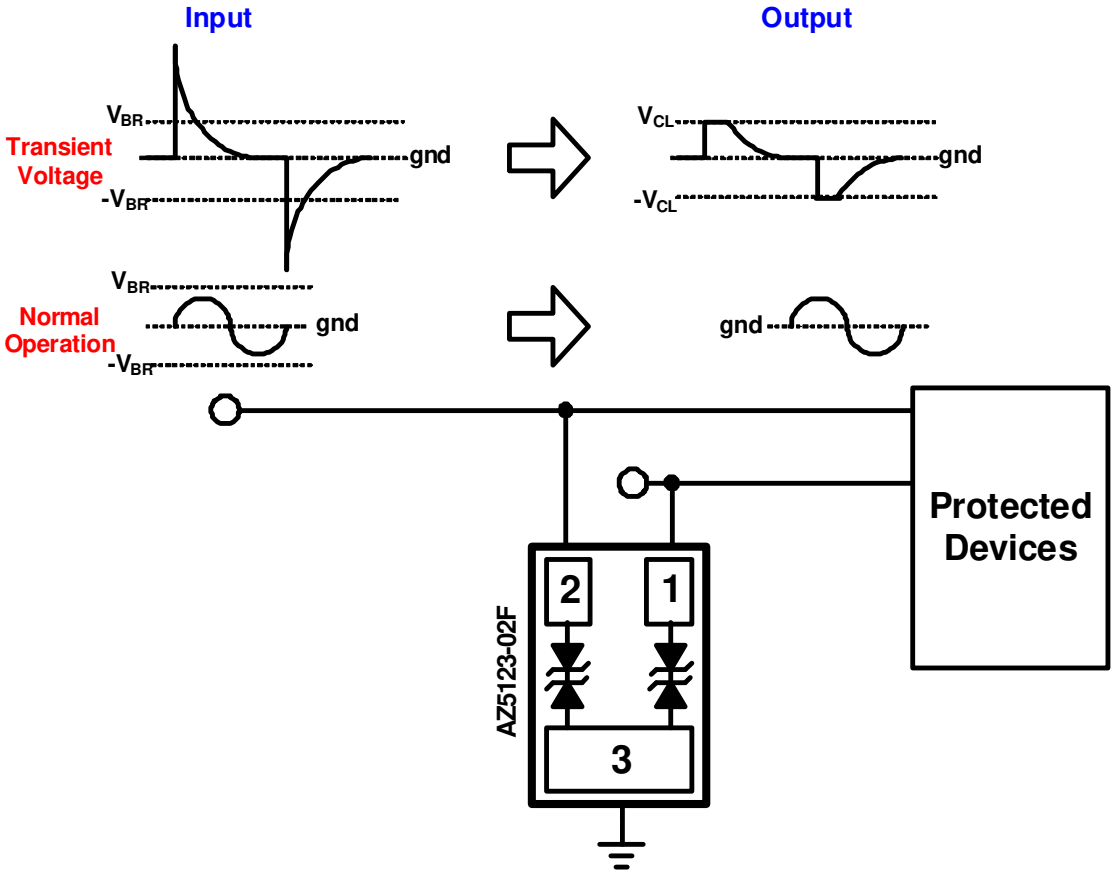
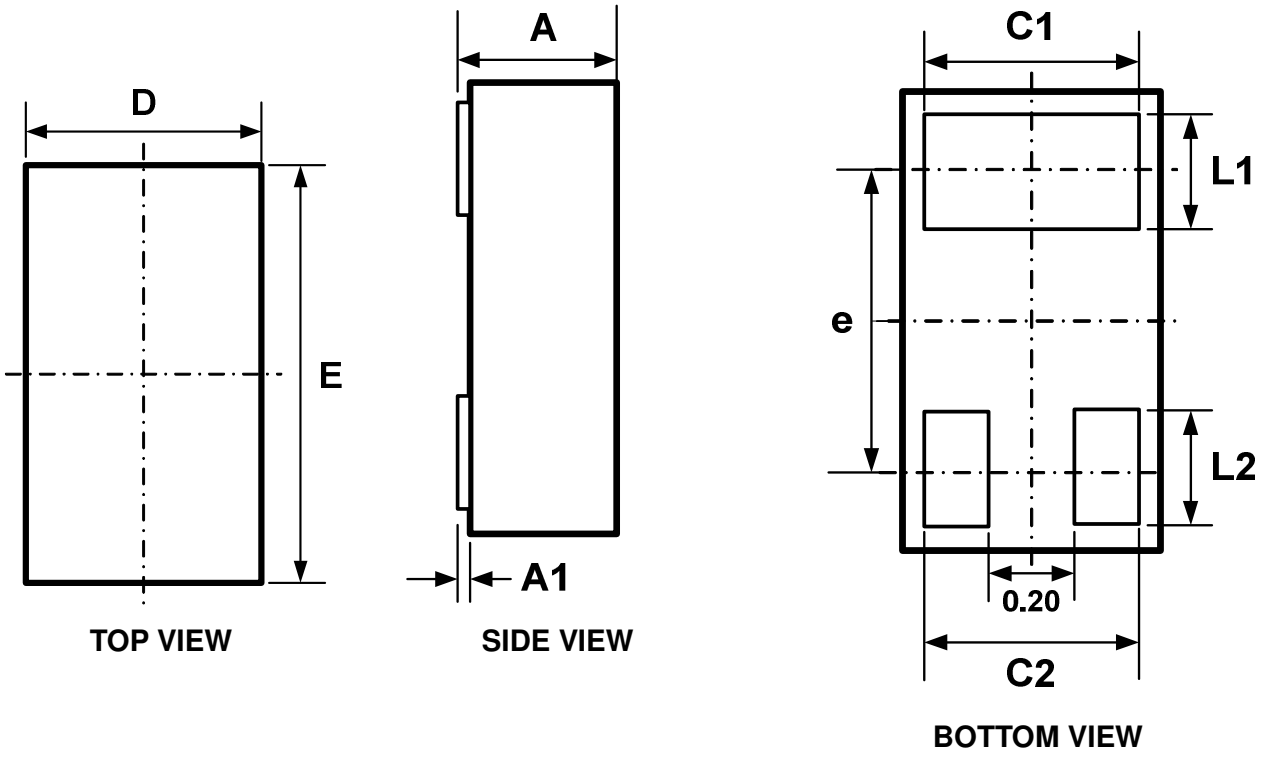


Fig. 1

Mechanical Details

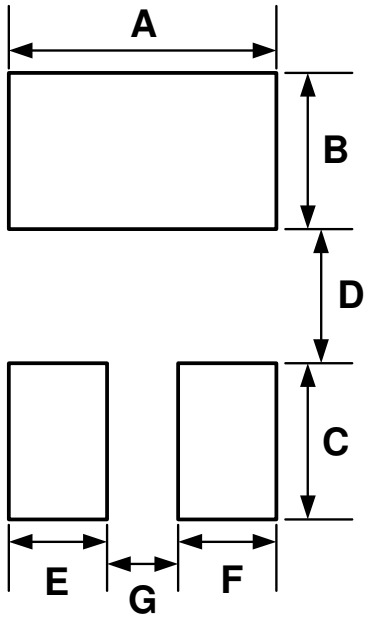
DFN1006P3X

PACKAGE DIAGRAMS AND DIMENSIONS



SYMBOL	MILLIMETERS			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
E	0.95	1.00	1.05	0.037	0.039	0.041
D	0.55	0.60	0.65	0.022	0.024	0.026
A	0.45	0.50	0.55	0.018	0.020	0.022
A1	0.00	0.02	0.05	0.000	0.001	0.002
C1	0.45	0.50	0.55	0.018	0.020	0.022
C2	0.45	0.50	0.55	0.018	0.020	0.022
L1	0.20	0.25	0.30	0.008	0.010	0.012
L2	0.20	0.25	0.30	0.008	0.010	0.012
e	0.65 BSC			0.026BSC		

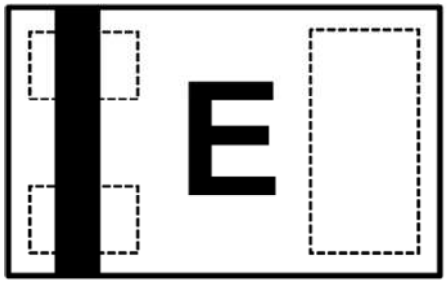
LAND LAYOUT



Dimensions		
Index	**Millimeter**	**Inches**
A	0.600	0.024
B	0.350	0.014
C	0.350	0.014
D	0.300	0.012
E	0.225	0.009
F	0.225	0.009
G	0.150	0.006

Notes:
This LAND LAYOUT is for reference purposes only. Please consult your manufacturing partners to ensure your company's PCB design guidelines are met.

MARKING CODE



Top View
E=device code

Part Number	Marking Code
AZ5123-02F.R7GR (Green part)	E

Note. Green means Pb-free, RoHS, and Halogen free compliant.

Ordering Information

PN#	Material	Type	Reel size	MOQ	MOQ/internal box	MOQ/carton
AZ5123-02F.R7GR	Green	T/R	7 inch	12,000/reel	4 reels=48,000/box	6 boxes=288,000/carton

Revision History

Revision	Modification Description
Revision 2015/04/30	Preliminary Release.
Revision 2018/03/14	1. Update the package dimensions. 2. Formal Release.