NTE7430
Integrated Circuit
TTL – 8–Input Positive NAND Gate

Description:
The NTE7430 contains a single 8–Input NAND gate in a 14–Lead plastic DIP type package.

Absolute Maximum Ratings: (Note 1)
Supply Voltage, V_{CC} 7V
DC Input Voltage, V_{IN} 5.5V
Operating Temperature Range, T_A . . . . 0°C to +70°C
Storage Temperature Range, T_{stg} . . . . −65°C to +150°C

Note 1. Unless otherwise specified, all voltages are referenced to GND.

Recommended Operating Conditions:

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.75	5.0	5.25	V
High−Level Input Voltage	V_{IH}	2.0	–	–	V
Low−Level Input Voltage	V_{IL}	–	–	0.8	V
High−Level Output Current	I_{OH}	–	–	−0.4	mA
Low−Level Output Current	I_{OL}	–	–	16	mA
Operating Temperature Range	T_A	0	–	+70	°C

Electrical Characteristics: (Note 2, Note 3)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Clamp Voltage	V_{IK}	V_{CC} = MIN, I_I = −12mA	–	–	−1.5	V
High Level Output Voltage	V_{OH}	V_{CC} = MIN, V_{IL} = 0.8V, I_{OH} = −0.4mA	2.4	3.4	–	V
Low Level Output Voltage	V_{OL}	V_{CC} = MIN, V_{IH} = 2V, I_{OL} = 16mA	–	0.2	0.4	V
Input Current	I_I	V_{CC} = MAX, V_I = 5.5V	–	–	1	mA

Note 2. .For conditions shown as MIN or MAX, use the appropriate value specified under "Recommended Operation Conditions".
Note 3. All typical values are at V_{CC} = 5V, T_A = +25°C.

Electrical Characteristics (Cont'd): (Note 2, Note 3)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
High Level Input Current	I_{IH}	V_{CC} = MAX, V_I = 2.4V	–	–	40	µA
Low Level Input Current	I_{IL}	V_{CC} = MAX, V_I = 0.4V	–	–	–1.6	mA
Short–Circuit Output Current	I_{OS}	V_{CC} = MAX, Note 4	–18	–	–55	mA
High Level Supply Current	I_{CCH}	V_{CC} = MAX, V_I = 0	–	1	2	mA
Low Level Supply Current	I_{CCL}	V_{CC} = MAX, V_I = 4.5V	–	3	6	mA

Note 2. .For conditions shown as MIN or MAX, use the appropriate value specified under "Recommended Operation Conditions".

Note 3. All typical values are at V_{CC} = 5V, T_A = +25°C.

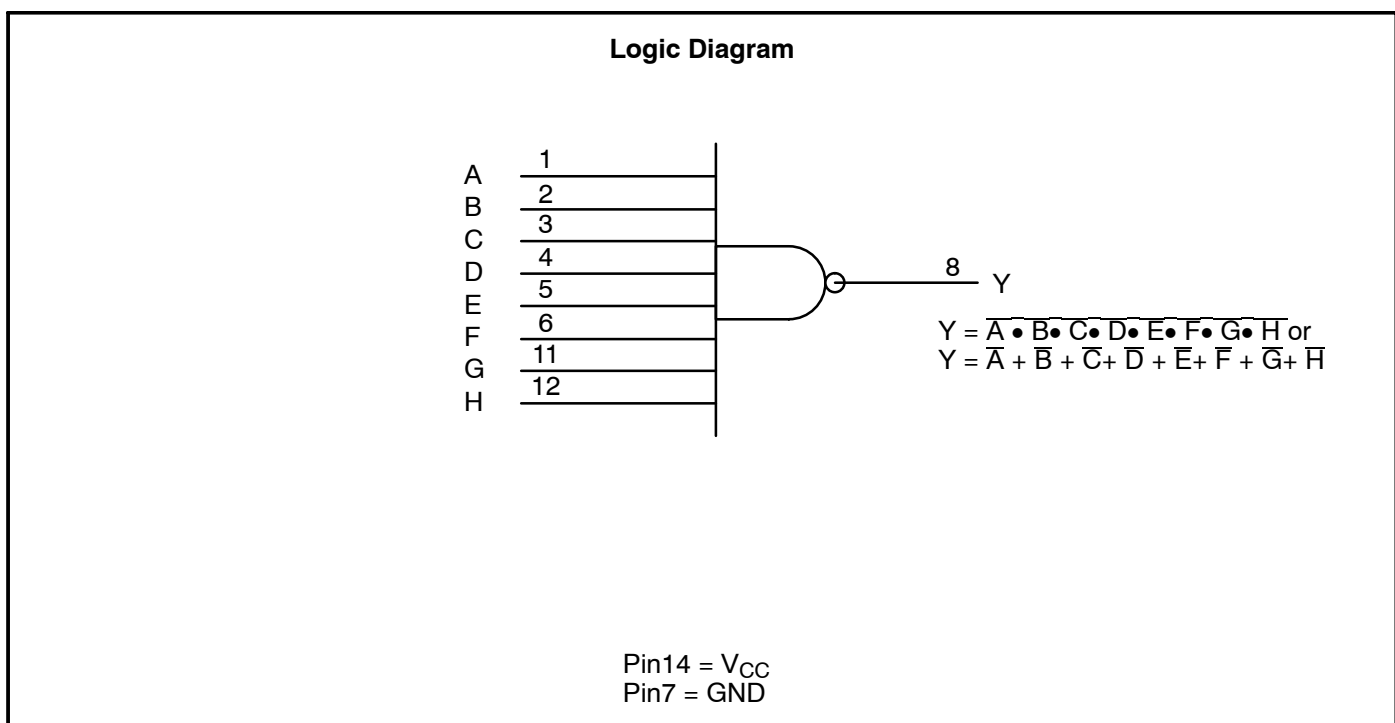Note 4. Not more than one output should be shorted at a time.

Switching Characteristics: (V_{CC} = 5V, T_A = +25°C unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Propagation Delay Time From Any Input to Y Output)	t_{PLH}	R_L = 400Ω, C_L = 15pF	–	13	22	ns
	t_{PHL}		–	8	15	ns

Function Table (Each Gate):

Inputs	Output
A thru H	**Y**
All Inputs H	L
One or More Inputs L	H

Logic Diagram

$Y = \overline{A \bullet B \bullet C \bullet D \bullet E \bullet F \bullet G \bullet H}$ or
$Y = \overline{A} + \overline{B} + \overline{C} + \overline{D} + \overline{E} + \overline{F} + \overline{G} + \overline{H}$

Pin14 = V_{CC}
Pin7 = GND

Pin Connection Diagram

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          ┌───┐  ┌───┐
    A  [1 ]│   └──┘   │[14]  V_CC
    B  [2 ]│          │[13]  N.C.
    C  [3 ]│          │[12]  H
    D  [4 ]│          │[11]  G
    E  [5 ]│          │[10]  N.C.
    F  [6 ]│          │[9 ]  N.C.
  GND  [7 ]│          │[8 ]  Y
          └──────────┘
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14   8

1   7

.785 (19.95) Max

.300 (7.62)

.200
(5.08)
Max

.100 (2.45)

.099 (2.5) Min

.600 (15.24)