ELECTRONICS, INC.
44 FARRAND STREET
BLOOMFIELD, NJ 07003
(973) 748–5089
http://www.nteinc.com

NTE4026B & NTE4033B
Integrated Circuit
CMOS, Decade Counter/Divider

Description:

The NTE4026B and NTE4033B each consist of a 5−stage Johnson counter and an output decoder in 16−Lead DIP type package which converts the Johnson code to a 7−segment decoded output for driving one stage in a numerical display

These devices are particularly advantageous in display applications where low power dissipation and/ or low package count are important.

Inputs common to both types are CLOCK, RESET, and CLOCK INHIBIT; common outputs are CARRY OUT and the seven decoded outputs (a, b, c, d, e, f, and g). Additional inputs and outputs for the NTE4026B include DISPLAY ENABLE input and DISPLAY ENABLE and UNGATED "C−SEGMENT" outputs. Signals peculiar to the NTE4033B are RIPPLE−BLANKING INPUT and LAMP TEST input and a RIPPLE−BLANKING OUTPUT.

A high RESET signal clears the decade counter to its zero count. The counter is advanced one count at the positive clock signal transition if the CLOCK INHIBIT signal is low. Counter advancement via the clocl line is inhibited when the CLOCK INHIBIT signal is high. The CLOCK INHIBIT signal can be used as a negative−edge clock if the clock line is held high. Antilock gating is provided on the Johnson counter, thus assuring proper counting sequence. The CARRY−OUT (C_{OUT}) signal completes one cycle every ten CLOCK INPUT cycles and is used to clock the succeeding decade directly in a multi−decade counting chain.

The seven decoded outputs (a, b, c, d, e, f, and g) illuminate the proper segments in a seven−segment display device used for representing the decimal numbers 0 to 9. The 7−segment outputs go high on selection in the NTE4033B; in the NTE4026B these outputs go high only when the DISPLAY ENABLEINPUT is high.

Features:

- Counter and 7−Segment Decoding in One Package
- Easily Interfaced with 7−Segment Display Types
- Fully Static Counter Operation: DC to 6MHz (Typ) at V_{DD} = 10V
- Ideal for Low−Power Displays
- Display Enable Output: NTE4026B
- "Ripple Blanking" and Lamp Test: NTE4033B
- 100% Tested for Quiescent Current at 20V
- Standardized, Symmetrical Output Characteristics
- 5V, 10V, and 15V Parametric Ratings
- Schmitt−Triggered Clock Inputs

Applications:

- Decade Counting 7−Segment Decimal Display
- Frequency Division 7−Segment Decimal Display
- Clocks, Watches, Timers (e.g. ÷60, ÷60, ÷12 Counter/Display)
- Counter/Display Driver for Meter Applications

Absolute Maximum Ratings:

DC Supply−Voltage Range (Voltages referenced to V_{SS}), V_{DD} . . . . −0.5 to +20V

Input Voltage Range, All Inputs . . . . −0.5 to V_{DD} +0.5V

DC Input Current, Any One Input . . . . ±10mA

Power Dissipation, P_D

T_A = −40° to +60°C 500mW

T_A = +60° to +85°C . . . . Derate Linearly at 12mW/°C to 200mW

Device Dissipation Per Output Transistor (T_A = −40° to +85°C) 100mW

Operating Temperature Range, T_A . . . . −40° to +85°C

Storage Temperature Range, T_{stg} . . . . −65° to +150°C

Lead Temperature, T_L

During Soldering, $^1/_{16}$” ±$^1/_{32}$” (1.59 ± 0.79mm) from case 10s max . . . . +265°C

Recommended Operating Conditions: (Note 1)

Parameter	Symbol	V_{DD}	Min	Max	Unit
Supply Voltage Range (T_A = −40° to +85°C)			3	18	V
Clock Input Frequency	f_{CL}	5	–	2.5	MHz
		10	–	5.5	MHz
		15	–	8.0	MHz
Colck Pulse Width	t_W	5	200	–	ns
		10	100	–	ns
		15	80	–	ns
Clock Rise & Fall Time	t_{rCL}, t_{fCL}	5, 10, 15	Unlimited		
Clock Inhibit Setup Time	t_s	5	200	–	ns
		10	50	–	ns
		15	30	–	ns
Reset Pulse Width	t_{RW}	5	200	–	ns
		10	100	–	ns
		15	50	–	ns
Reset Removal Time	t_{rem}	5	30	–	ns
		10	15	–	ns
		15	10	–	ns

Note 1. For maximum reliability, nominal operating conditions should be selected so that operation is always within the ranges outlined in the Recommended Operating Conditions.

Static Electrical Characteristics: (T_A = +25°C unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Quiescent Device Current	I_{DD}max	V_{IN} = 0.5V, V_{DD} = 5V	–	0.04	5.0	µA
		V_{IN} = 0.10V, V_{DD} = 10V	–	0.04	10.0	µA
		V_{IN} = 0.15V, V_{DD} = 15V	–	0.04	20.0	µA
		V_{IN} = 0.20V, V_{DD} = 20V	–	0.08	100.0	µA

Static Electrical Characteristics (Cont'd): (T_A = +25°C unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Output Low (Sink) Current	I_{OH}min	V_O = 0.4V, V_{IN} = 0.5V, V_{DD} = 5V	0.51	1.0	–	mA
		V_O = 0.5V, V_{IN} = 0.10V, V_{DD} = 10V	1.3	2.6	–	mA
		V_O = 1.5V, V_{IN} = 0.15V, V_{DD} = 15V	3.4	6.8	–	mA
Output High (Source) Current	I_{OH}min	V_O = 4.6V, V_{IN} = 0.5V, V_{DD} = 5V	–0.51	–1.0	–	mA
		V_O = 2.5V, V_{IN} = 0.5V, V_{DD} = 5V	–1.6	–3.2	–	mA
		V_O = 9.5V, V_{IN} = 0.10V, V_{DD} = 10V	–1.3	–2.6	–	mA
		V_O = 13.5V, V_{IN} = 0.15V, V_{DD} = 15V	–3.4	–6.8	–	mA
Output Voltage Low–Level	V_{OL}max	V_{IN} = 0.5V, V_{DD} = 5V	–	0	0.05	V
		V_{IN} = 0.10V, V_{DD} = 10V	–	0	0.05	V
		V_{IN} = 0.15V, V_{DD} = 15V	–	0	0.05	V
Output Voltage High–Level	V_{OH}min	V_{IN} = 0.5V, V_{DD} = 5V	4.95	5.0	–	V
		V_{IN} = 0.10V, V_{DD} = 10V	9.95	10.0	–	V
		V_{IN} = 0.15V, V_{DD} = 15V	14.95	15.0	–	V
Input Low Voltage	V_{IL}max	V_O = 0.5V to 4.5V, V_{DD} = 5V	–	–	1.5	V
		V_O = 1.9V, V_{DD} = 10V	–	–	3.0	V
		V_O = 1.5V to 13.5V, V_{DD} = 15V	–	–	4.0	V
Input High Voltage	V_{IH}min	V_O = 0.5V to 4.5V, V_{DD} = 5V	3.5	–	–	V
		V_O = 1.9V, V_{DD} = 10V	7.0	–	–	V
		V_O = 1.5V to 13.5V, V_{DD} = 15V	11.0	–	–	V
Input Current	I_{IN}max	V_{IN} = 0.18V, V_{DD} = 18V	–	$\pm10^{-5}$	±0.1	µA

Dynamic Electrical Characteristics: (T_A = +25°C, Input t_r, t_f = 20ns, C_L = 50pF, R_L = 200kΩ unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Clocked Operation						
Propagation Delay Time Decode Out	t_{PHL}, t_{PLH}	V_{DD} = 5V	–	350	700	ns
		V_{DD} = 10V	–	125	250	ns
		V_{DD} = 15V	–	90	180	ns
Carry Out		V_{DD} = 5V	–	250	500	ns
		V_{DD} = 10V	–	100	200	ns
		V_{DD} = 15V	–	75	150	ns
Transition Time, Carry Out Line	t_{THL}, t_{TLH}	V_{DD} = 5V	–	100	200	ns
		V_{DD} = 10V	–	50	100	ns
		V_{DD} = 15V	–	25	50	ns
Maximum Clock Input Frequency	f_{CL}	V_{DD} = 5V, Note 2	2.5	5.0	–	MHz
		V_{DD} = 10V, Note 2	5.5	11.0	–	MHz
		V_{DD} = 15V, Note 2	8.0	16.0	–	MHz

Note 2. Measured with respect to carry output line.

Dynamic Electrical Characteristics (Cont'd): (T_A = +25°C, Input t_r, t_f = 20ns, C_L = 50pF, R_L = 200kΩ unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Clocked Operation (Cont'd)						
Minimum Clock Pulse Width	t_W	V_{DD} = 5V	–	110	220	ns
		V_{DD} = 10V	–	50	100	ns
		V_{DD} = 15V	–	40	80	ns
Clock Rise or Fall Time	t_{rCL}, t_{fCL}	V_{DD} = 5V, 10V or 15V		Unlimited		
Minimum Clock Inhibit to Clock Setup Time	t_s	V_{DD} = 5V	–	115	230	ns
		V_{DD} = 10V	–	50	100	ns
		V_{DD} = 15V	–	30	70	ns
Average Input Capacitance	C_{IN}	Any Input	–	5	7	pF
Reset Operation						
Propagation Delay Time, To Carry Out Line	t_{PLH}	V_{DD} = 5V	–	275	550	ns
		V_{DD} = 10V	–	120	240	ns
		V_{DD} = 15V	–	80	160	ns
To Decode Out Lines	t_{PHL}, t_{PLH}	V_{DD} = 5V	–	300	600	ns
		V_{DD} = 10V	–	125	250	ns
		V_{DD} = 15V	–	90	180	ns
Minimum Reset Pulse Width	t_W	V_{DD} = 5V	–	100	120	ns
		V_{DD} = 10V	–	50	100	ns
		V_{DD} = 15V	–	25	50	ns
Minimum Reset Removal Time		V_{DD} = 5V	–	0	30	ns
		V_{DD} = 10V	–	0	15	ns
		V_{DD} = 15V	–	0	10	ns

Application Notes:

NTE4026B

When the DISPLAY ENABLE INPUT is low the seven decoded outputs are forced low regardless of the state of the counter. Activation of the display only when required results in significant power savings. This system also facilitates implementation of display−character multiplexing.

The CARRY OUT and UNGATED "C−SEGMENT" signals are not gated by the DISPLAY ENABLE and therefore are available continuously. This feature is a requirement in implementation of certain divider functions such as divide−by−60 and divide−by−12.

NTE4033B

The NTE4033B has provisions for automatic blanking of the non−significant zeros in a multi−digit decimal number which results in an easily readable display consistent with normal writing practice. For example, the number 0050.0700 in an eight digit display would be displayed as 50.07. Zero suppression on the integer side is obtained by connecting the RBI pin of the NTE4033B associated with the most significant digit in the display to a low−level voltage and connecting the RBO pin of that stage to the RBI pin of the NTE4033B in the next−lower significant position in the display. This procedure is continued for each succeeding NTE4033B on the integer side of the display

Application Notes (Cont'd):

NTE4033B

On the fraction side of the display the RBI of the NTE4033B associated with the least significant bit is connected to a low−level voltage and the RBO of that NTE4033B is connected to the RBI pin of the NTE4033B in the next more−significant−bit position. Again, this procedure is continued for all NTE4033B's on the fraction side of the display.

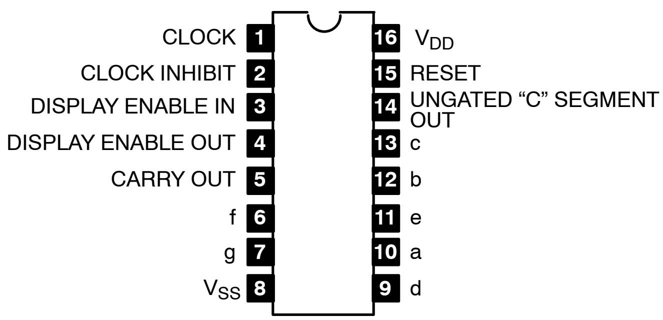
In a purely fractional number the zero immediately preceding the decimal point can be displayed by connecting the RBI of that stage to a high level voltage (instead of to the RBO of the next more−significant−stage). For example: optional zero → 0.7346. Likewise, the zero in a number such as 763.0 can be displayed by connecting the RBI of the NTE4033B associated with it to a high−level voltage.

Ripple blanking of non−significant zeros provides an appreciable savings in display power.

The NTE4033B has a LAMP TEST input which when connected to a high−level voltage, overrides normal decoder operation and enables a check to be made on possible display malfunctions by putting the seven outputs in the high state.

Pin Connection Diagram

NTE4026B



NTE4033B