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NTD80N02

Power MOSFET

24 V, 80 A, N-Channel DPAK

Designed for low voltage, high speed switching applications in power supplies, converters and power motor controls and bridge circuits.

Features

- These Devices are Pb-Free and are RoHS Compliant

Typical Applications

- Power Supplies
- Converters
- Power Motor Controls
- Bridge Circuits

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain-to-Source Voltage	V _{DSS}	24	Vdc
Gate-to-Source Voltage - Continuous	V _{GS}	±20	Vdc
Drain Current - Continuous @ T _C = 25°C - Single Pulse (t _p = 10 μs)	I _D I _{DM}	80* 200	Adc
Total Power Dissipation @ T _C = 25°C	P _D	75	Watts
Operating and Storage Temperature Range	T _J , T _{stg}	-55 to 150	°C
Single Pulse Drain-to-Source Avalanche Energy - Starting T _J = 25°C (V _{DD} = 24 Vdc, V _{GS} = 10 Vdc, I _L = 17 Apk, L = 5.0 mH, R _G = 25 Ω)	E _{AS}	733	mJ
Thermal Resistance - Junction-to-Case - Junction-to-Ambient (Note 1) - Junction-to-Ambient (Note 2)	R _{θJC} R _{θJA} R _{θJA}	1.65 67 120	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8" from case for 10 seconds	T _L	260	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. When surface mounted to an FR4 board using 1" pad size, (Cu Area 1.127 in²).
2. When surface mounted to an FR4 board using the minimum recommended pad size, (Cu Area 0.412 in²).

*Chip current capability limited by package.

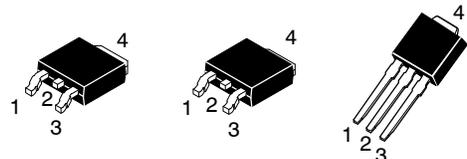
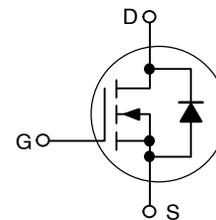


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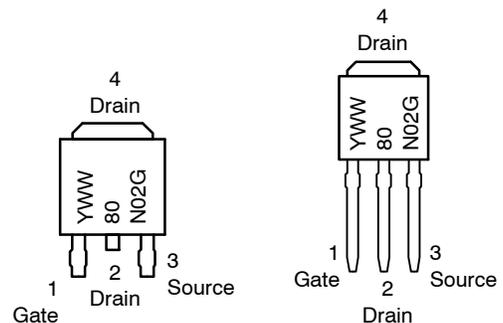
V _{(BR)DSS}	R _{DS(on)} TYP	I _D MAX
24 V	5.0 mΩ	80 A

N-Channel



CASE 369AA DPAK (Surface Mount) **STYLE 2**
CASE 369C DPAK (Surface Mount) **STYLE 2**
CASE 369D DPAK (Straight Lead) **STYLE 2**

MARKING DIAGRAMS & PIN ASSIGNMENTS



80N02 = Device Code
 Y = Year
 WW = Work Week
 G = Pb-Free Package

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 5 of this data sheet.

NTD80N02

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage (Note 3) (V _{GS} = 0 Vdc, I _D = 250 μAdc) Positive Temperature Coefficient	V _{(BR)DSS}	24 -	27 25	- -	Vdc mV/°C
Zero Gate Voltage Drain Current (V _{GS} = 0 Vdc, V _{DS} = 24 Vdc) (V _{GS} = 0 Vdc, V _{DS} = 24 Vdc, T _J = 125°C)	I _{DSS}	- -	- -	1.0 10	μAdc
Gate-Body Leakage Current (V _{GS} = ±20 Vdc, V _{DS} = 0 Vdc)	I _{GSS}	-	-	±100	nAdc

ON CHARACTERISTICS (Note 3)

Gate Threshold Voltage (Note 3) (V _{DS} = V _{GS} , I _D = 250 μAdc) Negative Threshold Temperature Coefficient	V _{GS(th)}	1.0 -	1.9 -3.8	3.0 -	Vdc mV/°C
Static Drain-to-Source On-Resistance (Note 3) (V _{GS} = 10 Vdc, I _D = 80 Adc) (V _{GS} = 4.5 Vdc, I _D = 40 Adc) (V _{GS} = 10 Vdc, I _D = 20 Adc) (V _{GS} = 4.5 Vdc, I _D = 20 Adc)	R _{DS(on)}	- - - -	5.0 7.5 5.0 7.5	5.8 9.0 5.8 9.0	mΩ
Forward Transconductance (V _{DS} = 15 Vdc, I _D = 10 Adc) (Note 3)	g _{FS}	-	20	-	Mhos

DYNAMIC CHARACTERISTICS

Input Capacitance	(V _{DS} = 20 Vdc, V _{GS} = 0 V, f = 1.0 MHz)	C _{ISS}	-	2250	2600	pF
Output Capacitance		C _{OSS}	-	900	1100	
Transfer Capacitance		C _{rSS}	-	400	525	

SWITCHING CHARACTERISTICS (Note 4)

Turn-On Delay Time	(V _{GS} = 4.5 Vdc, V _{DD} = 20 Vdc, I _D = 20 Adc, R _G = 2.5 Ω)	t _{d(on)}	-	17	30	ns
Rise Time		t _r	-	67	125	
Turn-Off Delay Time		t _{d(off)}	-	28	45	
Fall Time		t _f	-	40	75	
Gate Charge	(V _{GS} = 4.5 Vdc, I _D = 20 Adc, V _{DS} = 20 Vdc) (Note 3)	Q _T	-	30	42	nC
		Q ₁	-	7.0	12	
		Q ₂	-	18	28	

SOURCE-DRAIN DIODE CHARACTERISTICS

Forward On-Voltage (I _S = 20 Adc, V _{GS} = 0 Vdc) (Note 3) (I _S = 40 Adc, V _{GS} = 0 Vdc) (I _S = 20 Adc, V _{GS} = 0 Vdc, T _J = 150°C)	V _{SD}	- - -	0.92 1.05 0.70	1.2 - -	Vdc	
Reverse Recovery Time	(I _S = 20 Adc, V _{GS} = 0 Vdc, dI _S /dt = 100 A/μs) (Note 3)	t _{rr}	-	38	52	ns
		t _a	-	20	-	
		t _b	-	18	-	
Reverse Recovery Stored Charge	Q _{rr}	-	0.038	-	μC	

- Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
- Switching characteristics are independent of operating junction temperatures.

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TYPICAL CHARACTERISTICS

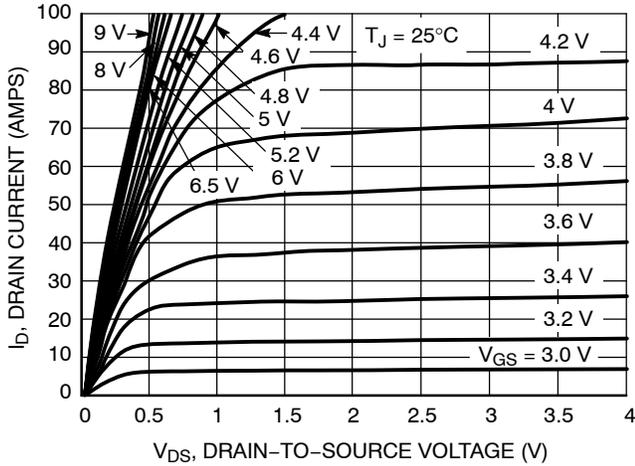


Figure 1. On-Region Characteristics

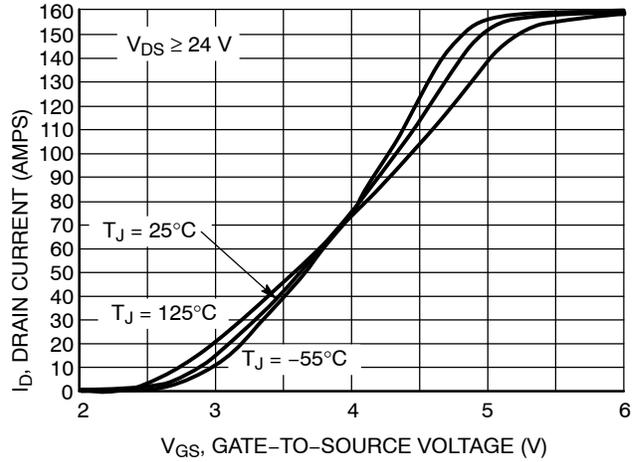


Figure 2. Transfer Characteristics

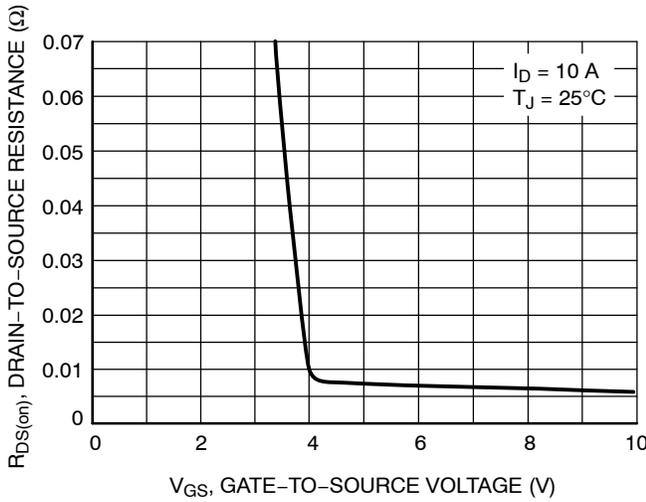


Figure 3. On-Resistance versus Gate-to-Source Voltage

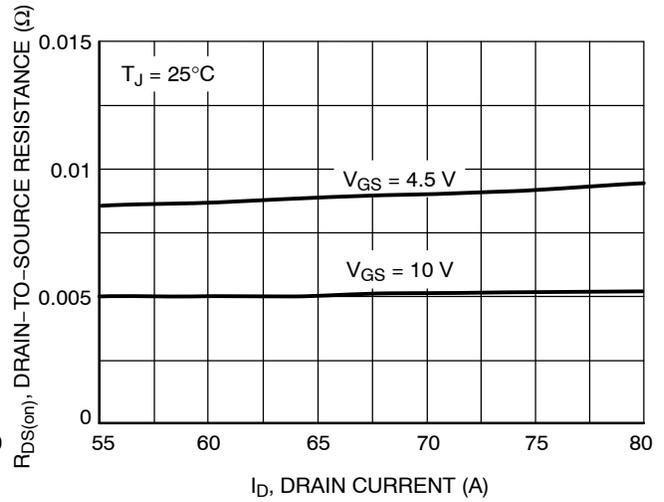


Figure 4. On-Resistance versus Drain Current and Gate Voltage

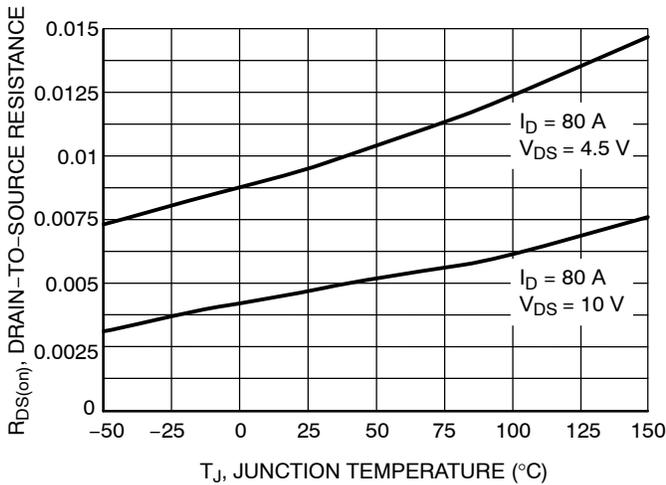


Figure 5. On-Resistance Variation with Temperature

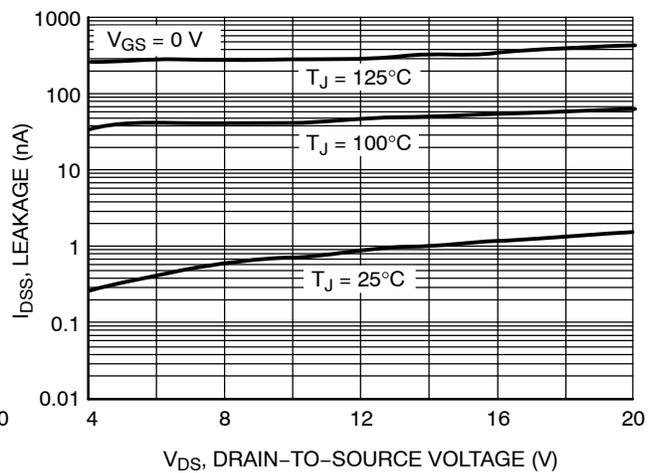


Figure 6. Drain-to-Source Leakage Current versus Voltage

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TYPICAL CHARACTERISTICS

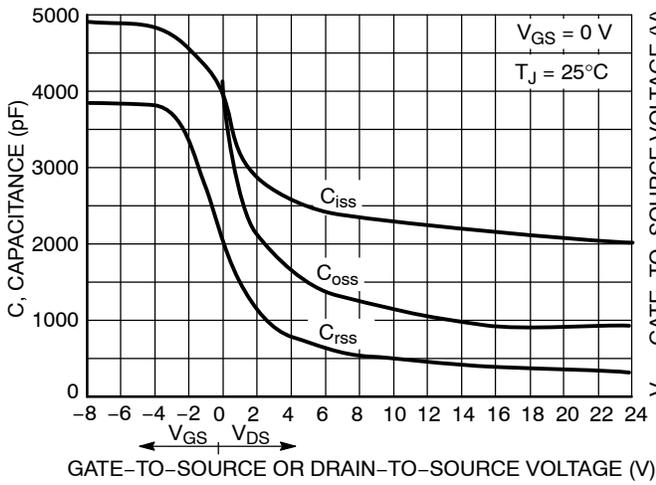


Figure 7. Capacitance Variation

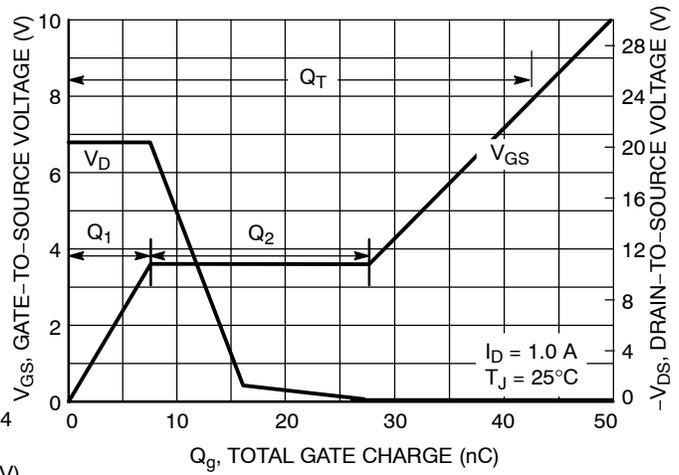


Figure 8. Gate-to-Source and Drain-to-Source Voltage versus Total Charge

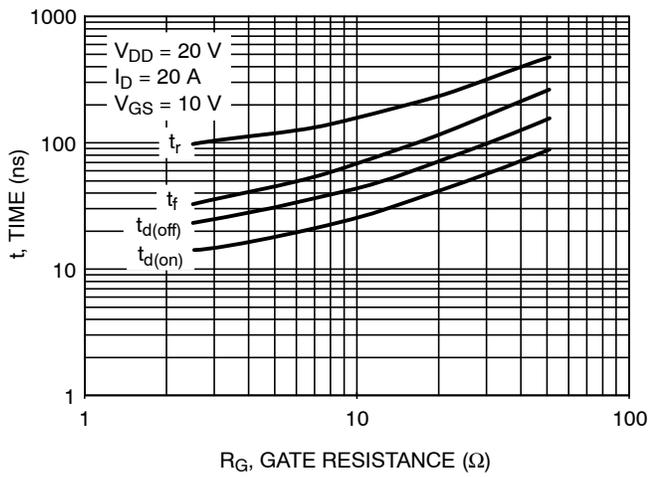


Figure 9. Resistive Switching Time Variation versus Gate Resistance

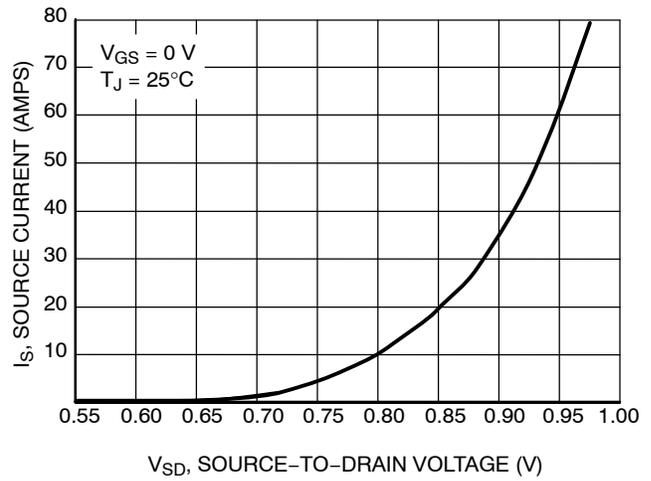


Figure 10. Diode Forward Voltage versus Current

NTD80N02

TYPICAL CHARACTERISTICS

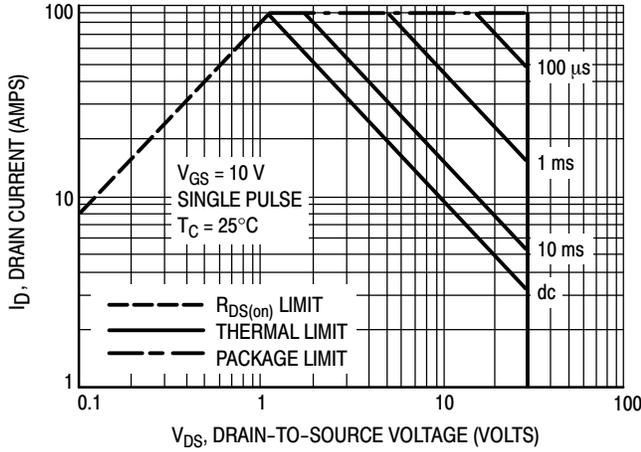


Figure 11. Maximum Rated Forward Biased Safe Operating Area

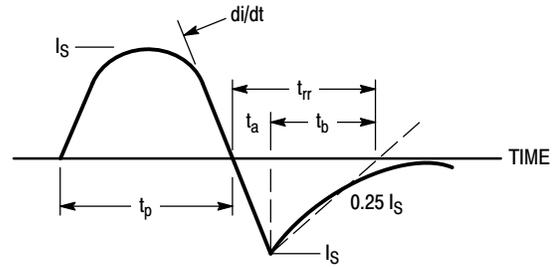


Figure 12. Diode Reverse Recovery Waveform

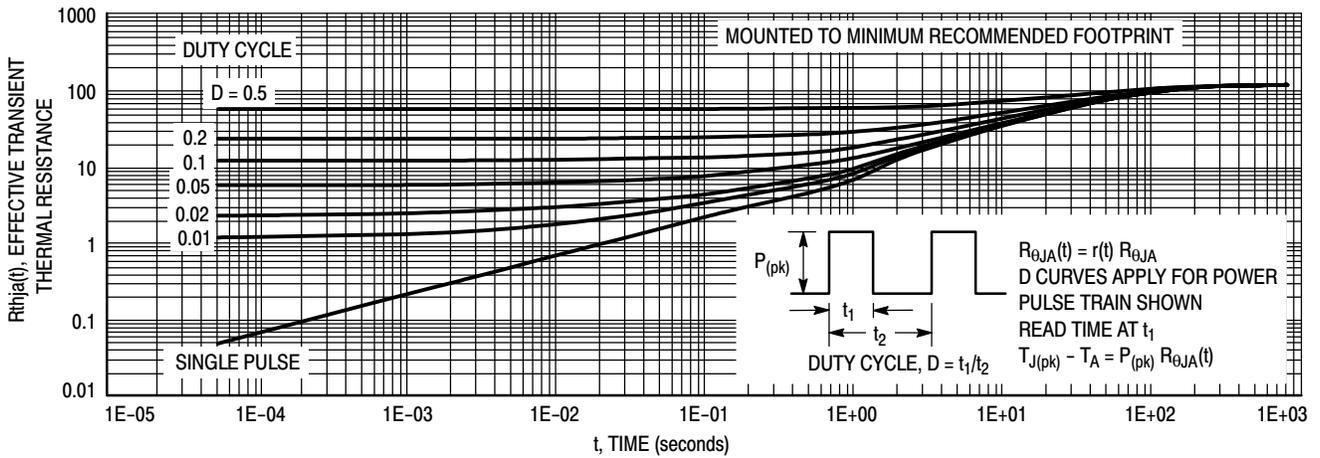


Figure 13. Thermal Response - Various Duty Cycles

ORDERING INFORMATION

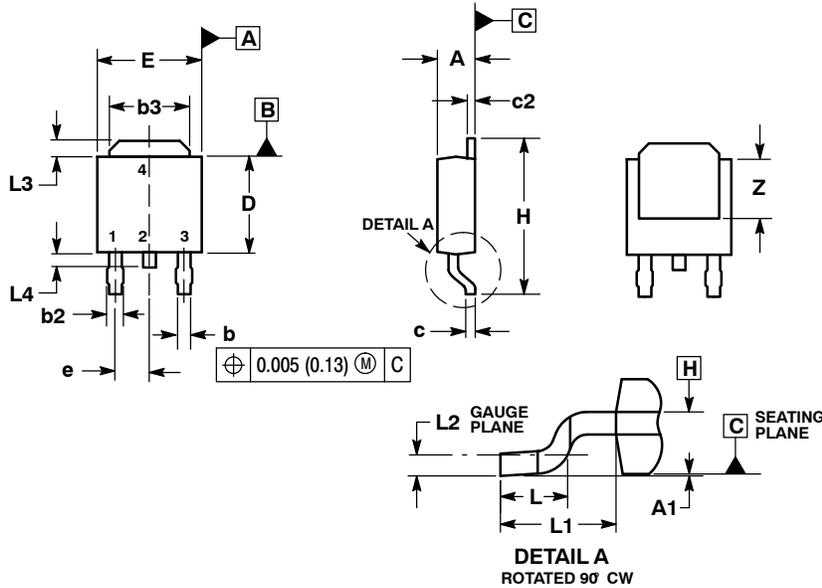
Order Number	Package	Shipping†
NTD80N02T4G	DPAK-3 (Pb-Free)	2500 / Tape & Reel
NTD80N02-1G	DPAK-3 Straight Lead (Pb-Free)	75 Units / Rail

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

NTD80N02

PACKAGE DIMENSIONS

DPAK (SINGLE GAUGE) CASE 369AA-01 ISSUE B

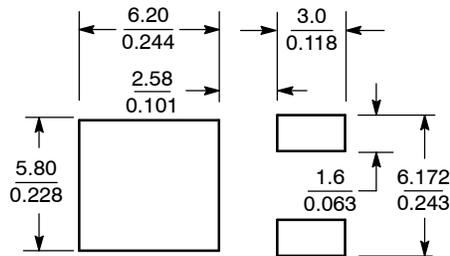


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCHES.
3. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS b3, L3 and Z.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.006 INCHES PER SIDE.
5. DIMENSIONS D AND E ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
6. DATUMS A AND B ARE DETERMINED AT DATUM PLANE H.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.086	0.094	2.18	2.38
A1	0.000	0.005	0.00	0.13
b	0.025	0.035	0.63	0.89
b2	0.030	0.045	0.76	1.14
b3	0.180	0.215	4.57	5.46
c	0.018	0.024	0.46	0.61
c2	0.018	0.024	0.46	0.61
D	0.235	0.245	5.97	6.22
E	0.250	0.265	6.35	6.73
e	0.090 BSC		2.29 BSC	
H	0.370	0.410	9.40	10.41
L	0.055	0.070	1.40	1.78
L1	0.108 REF		2.74 REF	
L2	0.020 BSC		0.51 BSC	
L3	0.035	0.050	0.89	1.27
L4	---	0.040	---	1.01
Z	0.155	---	3.93	---

SOLDERING FOOTPRINT*



SCALE 3:1 $\left(\frac{\text{mm}}{\text{inches}}\right)$

STYLE 2:

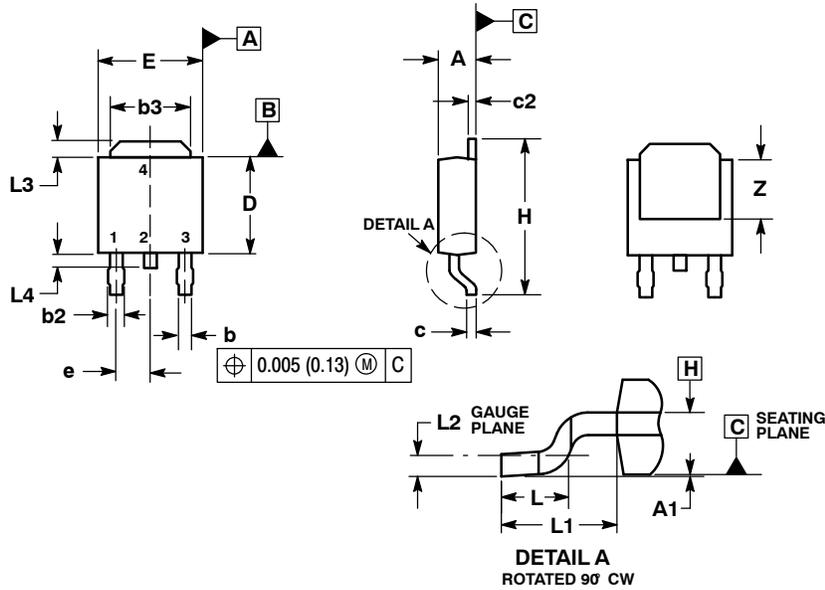
- PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

NTD80N02

PACKAGE DIMENSIONS

DPAK (SINGLE GAUGE) CASE 369C-01 ISSUE D



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCHES.
3. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS b3, L3 and Z.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.006 INCHES PER SIDE.
5. DIMENSIONS D AND E ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
6. DATUMS A AND B ARE DETERMINED AT DATUM PLANE H.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.086	0.094	2.18	2.38
A1	0.000	0.005	0.00	0.13
b	0.025	0.035	0.63	0.89
b2	0.030	0.045	0.76	1.14
b3	0.180	0.215	4.57	5.46
c	0.018	0.024	0.46	0.61
c2	0.018	0.024	0.46	0.61
D	0.235	0.245	5.97	6.22
E	0.250	0.265	6.35	6.73
e	0.090 BSC		2.29 BSC	
H	0.370	0.410	9.40	10.41
L	0.055	0.070	1.40	1.78
L1	0.108 REF		2.74 REF	
L2	0.020 BSC		0.51 BSC	
L3	0.035	0.050	0.89	1.27
L4	---	0.040	---	1.01
Z	0.155	---	3.93	---

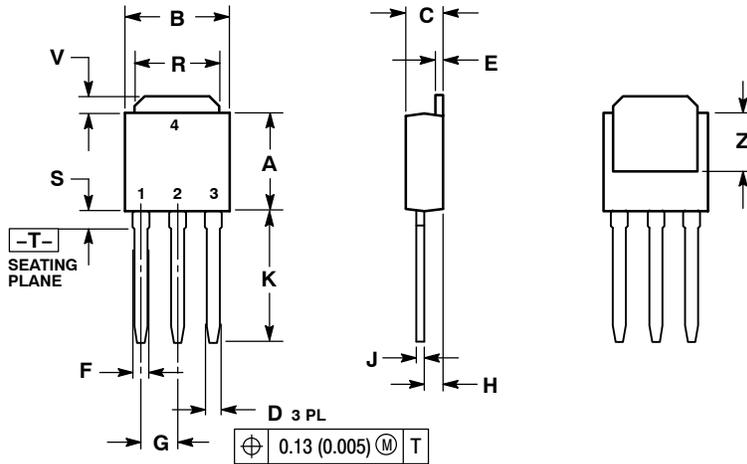
STYLE 2:

- PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

NTD80N02

PACKAGE DIMENSIONS

DPAK CASE 369D-01 ISSUE B



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.235	0.245	5.97	6.35
B	0.250	0.265	6.35	6.73
C	0.086	0.094	2.19	2.38
D	0.027	0.035	0.69	0.88
E	0.018	0.023	0.46	0.58
F	0.037	0.045	0.94	1.14
G	0.090 BSC		2.29 BSC	
H	0.034	0.040	0.87	1.01
J	0.018	0.023	0.46	0.58
K	0.350	0.380	8.89	9.65
R	0.180	0.215	4.45	5.45
S	0.025	0.040	0.63	1.01
V	0.035	0.050	0.89	1.27
Z	0.155	---	3.93	---

STYLE 2:

- PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

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